HY3123

Datasheet

Impedance Converter With 24-Bit ΣΔADC

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1. Feature

- AC Impedance converter
  - Built-in HAO(High Accuracy RC Oscillator), The selectable Frequency is : 2MHz, 4MHz, 8MHz; and also provide frequency output function
  - VDDA driving ability up to 10mA
  - Sinewave signal output with adjustable frequency and amplitude
  - Three Rail-to-rail OPAMP.
  - AC Impedance measurement circuit
  - 1Mhz, 24-bit ΣΔADC
  - I²C digital interface
- Operation environment
  - Digital voltage: 2.2V to 5.5V
  - Analog voltage: 2.2V to 3.6V
  - Operation temp.: –40°C to +85°C
- 24-bits ΣΔADC
  - Optional gains of: ×1/4, ×1/2, ×1~×16
  - Optional different data conversion output rate with upper limit of 31.25Ksps
  - Embedded DC bias voltage design
  - IRQ function
- 12-bit Resistor Ladder DAC
  - Programmable resistance voltage divider
  - Can be designed as a dual CH. 12-bit DAC with OPAMP
- Rail-to-Rail OPAMP
  - Internal three Rail-to-rail OPAMP
  - 1mA source and sink current
- Internal linear regulator VDDA and reference voltage REFO
  - VDDA output voltage: 2.2V~3.6V
  - REFO output voltage:1.2V
- I²C interface
  - Support standard communication format
  - F_{SCL} = 400KHz
  - Sleep function (for register control)
- IRQ PIN support
- BIA Module
  - Electrochemical Analysis
  - Bioelectrical Impedance Analysis
  - AC waveform frequency: 122Hz~250KHz
  - Impendence Range: 1K ~ 1MΩ
  - Phase detector: 0~90°
- Package
  - SSOP20
  - SSOP16

Function List

Model No.	VDD (V)	Internal Clock (Hz)	System Clock (Hz)	ADC ENOB (bit x ch)	Sample Rate (sps)	TPS	OPAMP (type x ch.)	DAC (bit x ch.)	Wavefor Genarator	IRQ Function	Serial Interface	Package
HY3123	2.2~5.5	2M 4M 8M	2M~8M	19-bit x 11	8~31.25K	yes	R2R x 3	12-bit x 2	yes	yes	I²C x 1	SSOP20 SSOP16

2. Product Overview

2.1. Function Block Diagram

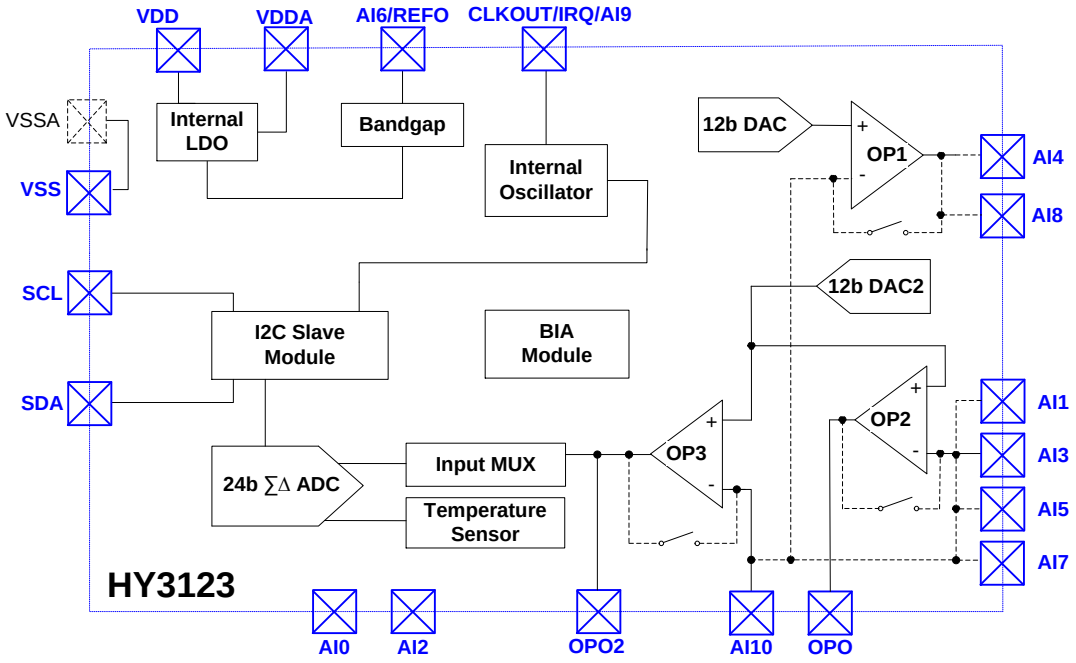


Figure 2-1 Block Diagram

2.2. Power System

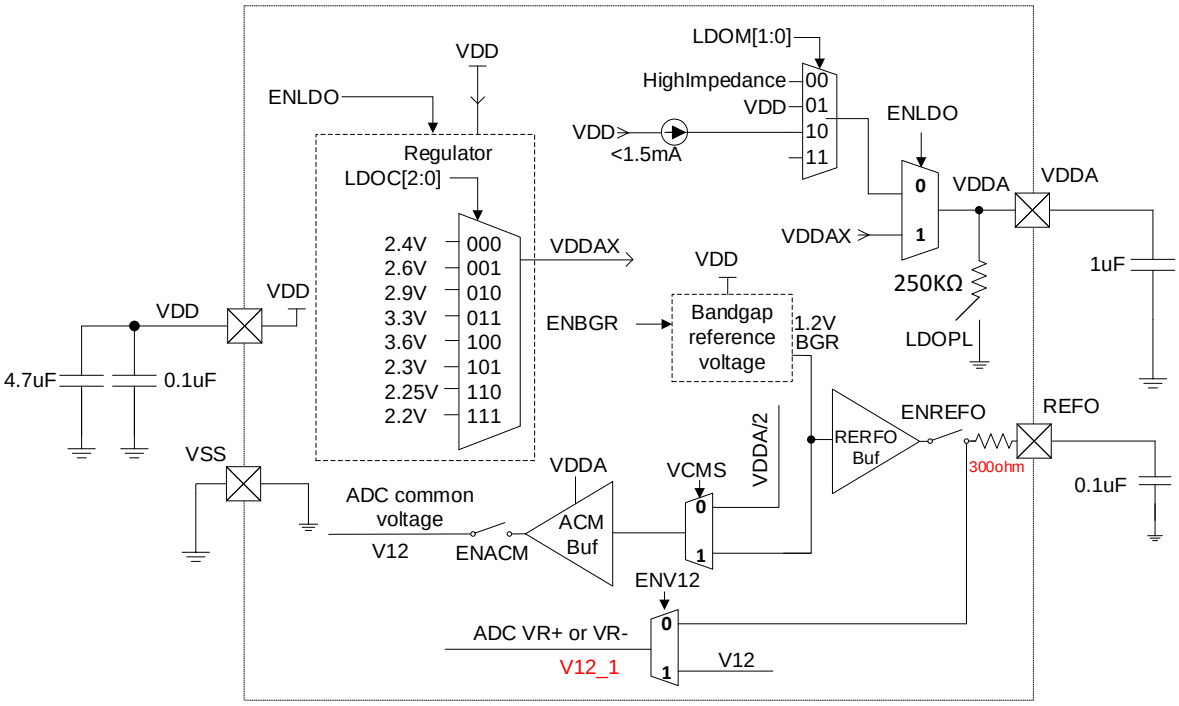


Figure 2-2 Power System Block

2.3. GPIO PORT CLKOUT/IRQ/AI9

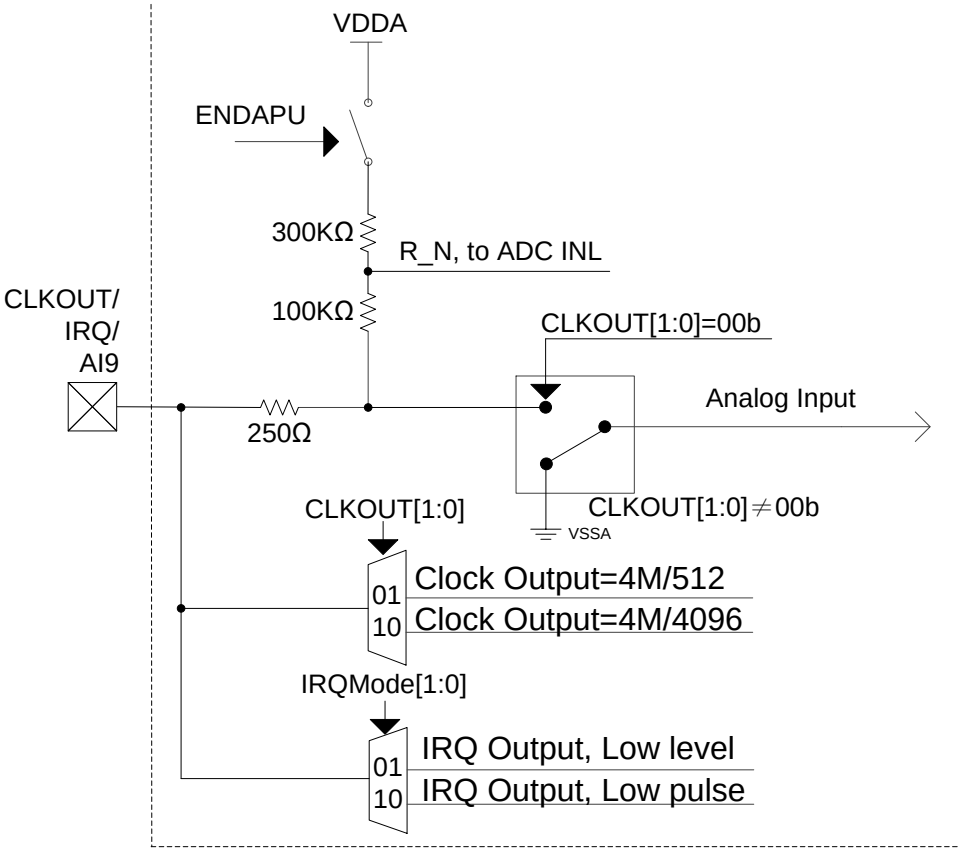


Figure 2-3 GPIO PORT CLKOUT/IRQ/AI9

2.4. 12-bit DAC I

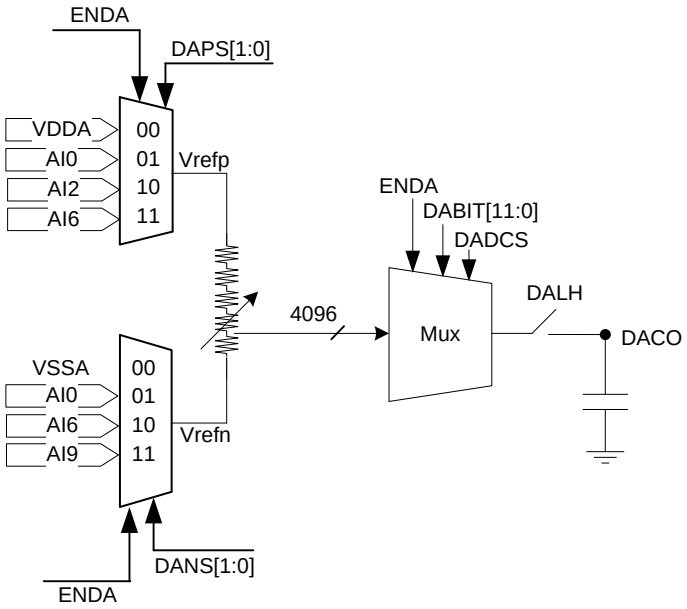


Figure 2-1 12-bit DAC I Block

2.5. 12-bit DAC II

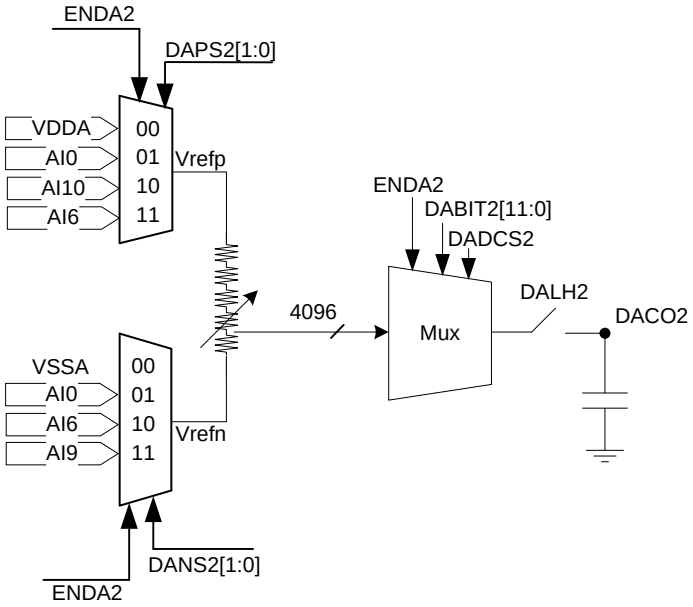


Figure 2-5 12-bit DAC II Block

2.6. Rail to Rail OPAMP1

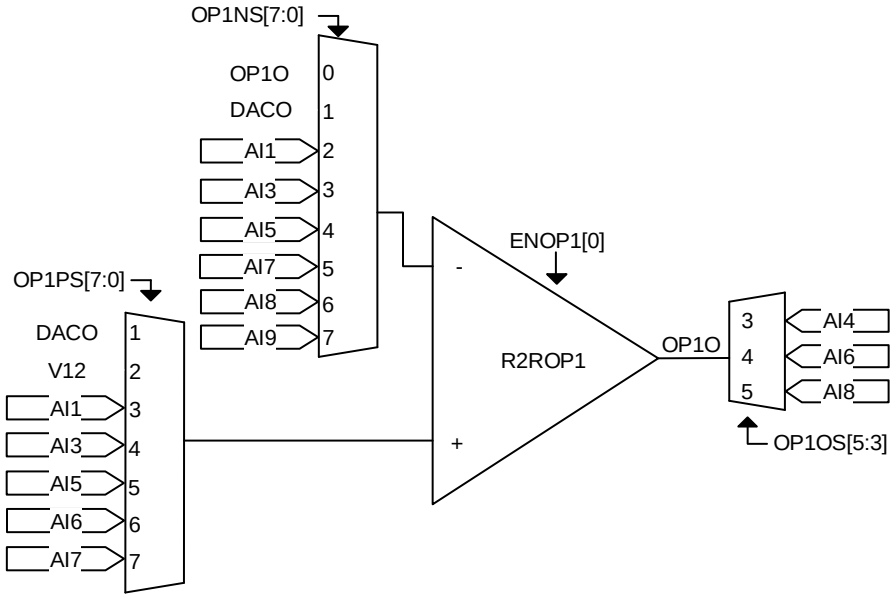


Figure 2-6 Rail to Rail OPAMP1 Block

2.7. Rail to Rail OPAMP2

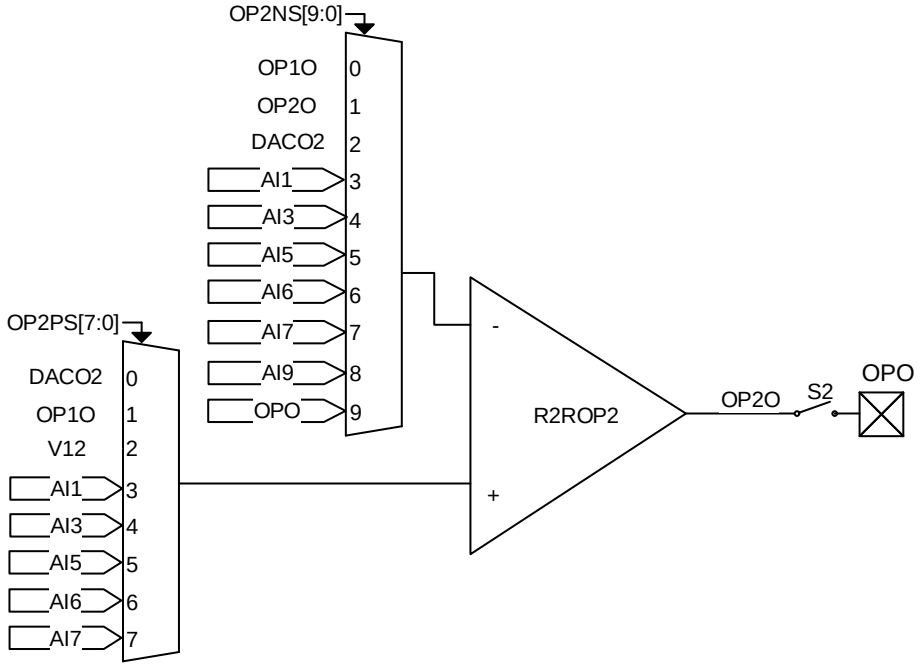


Figure 2-7 Rail to Rail OPAMP2 Block

2.8. Rail to Rail OPAMP3

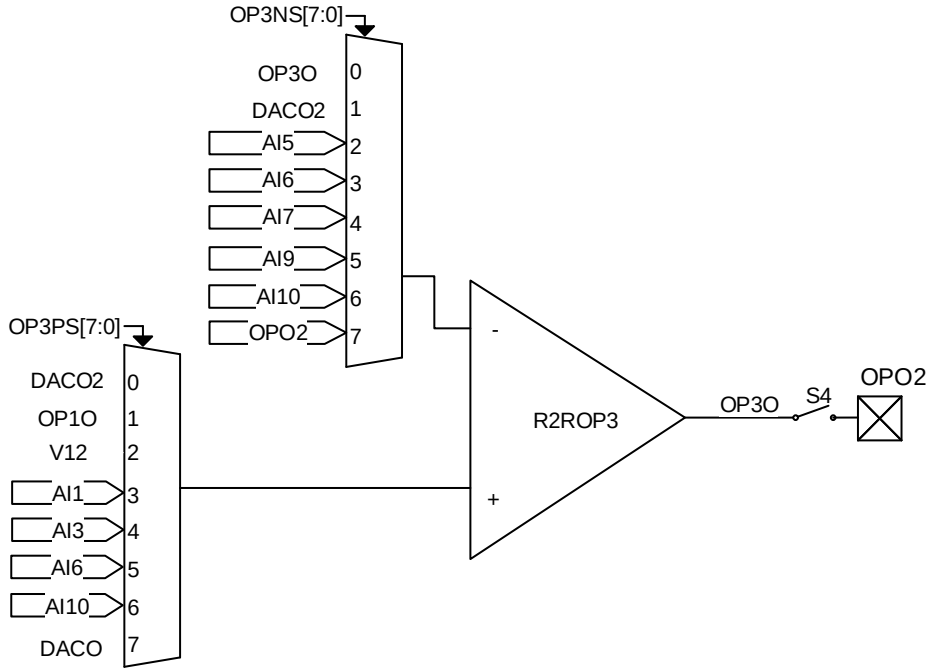


Figure 2-8 Rail to Rail OPAMP3 Block

2.9. 24-bit ∑ΔADC

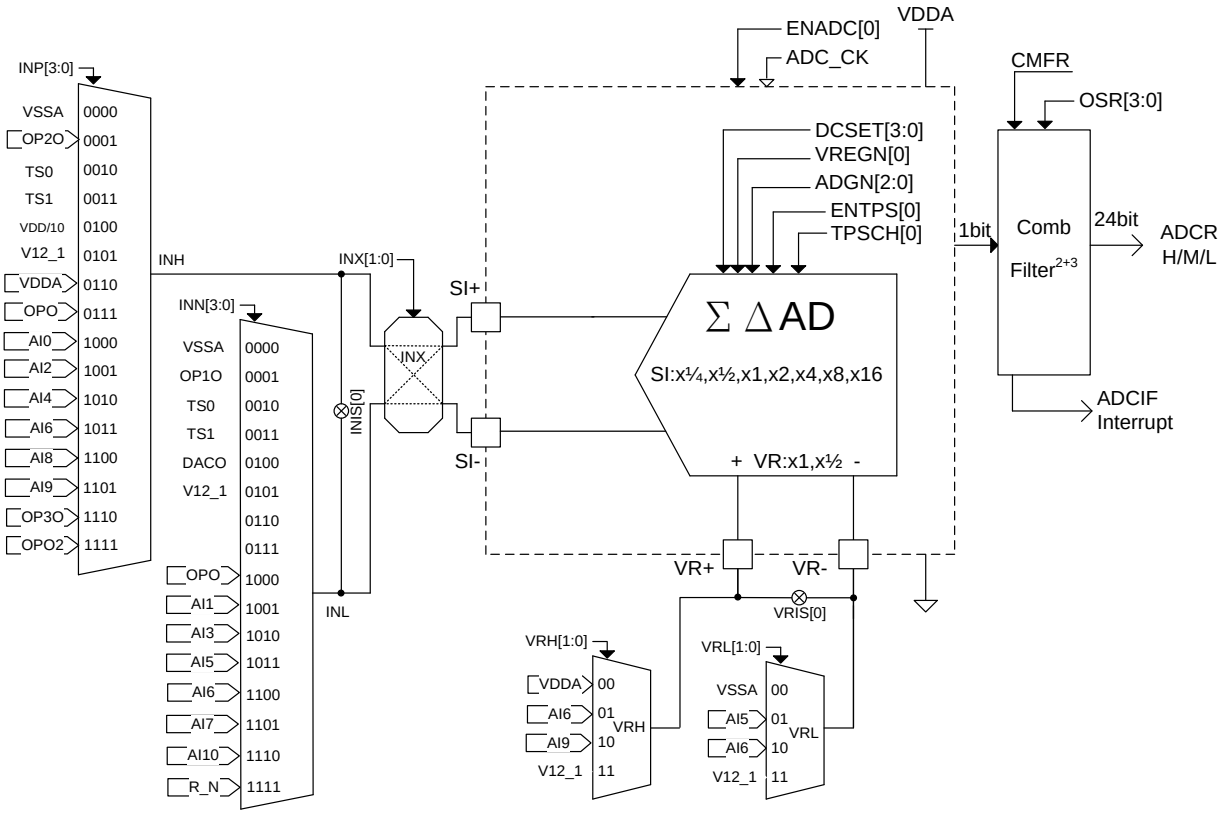


Figure 2-9 24-bit ∑ΔADC Block

2.10. BIA Module

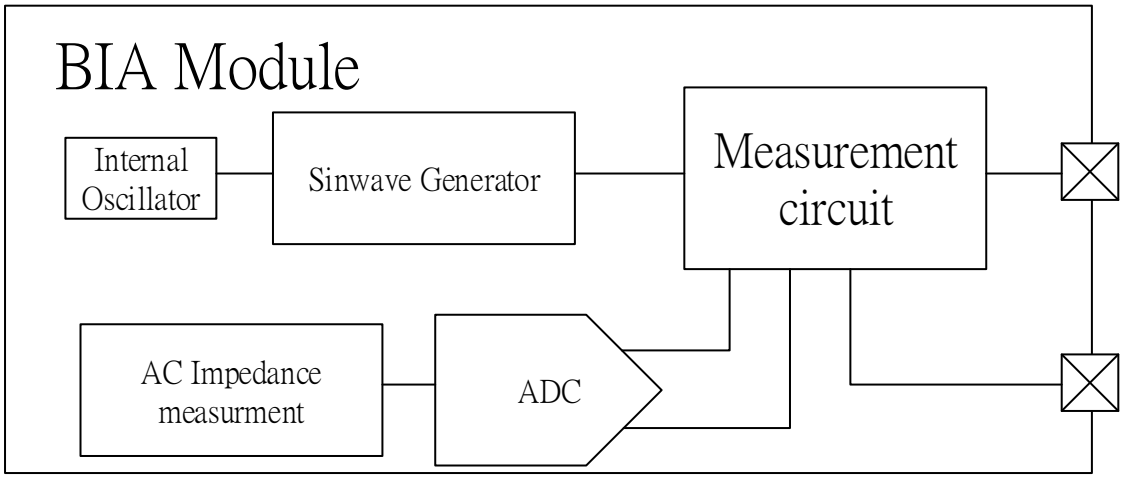


圖 2-10 BIA Block

※ For detailed information on BIA Module, please contact the HYCON Technology contact window.

3. Pin Definition

3.1. Product Pin Diagram

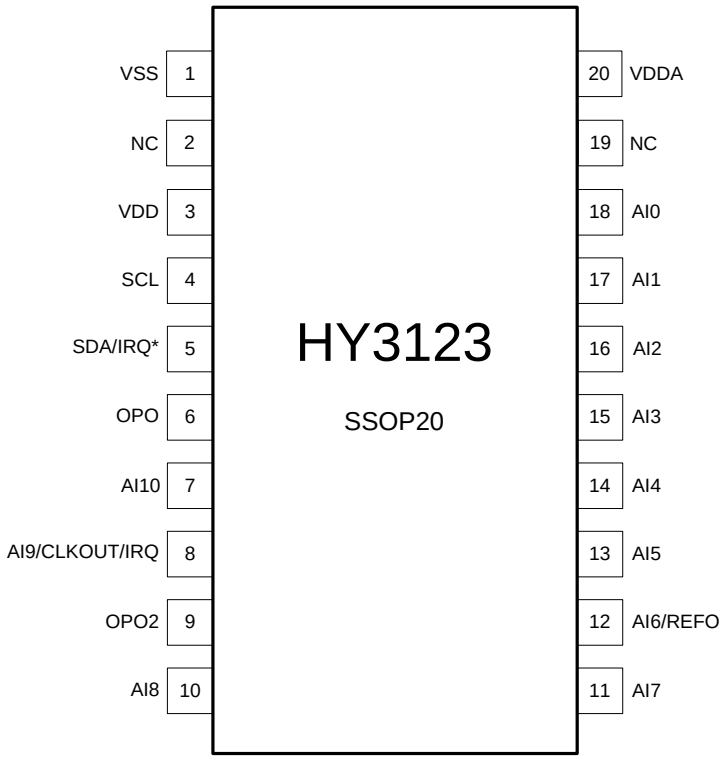


Figure 3-1 SSOP20 Pin Diagram

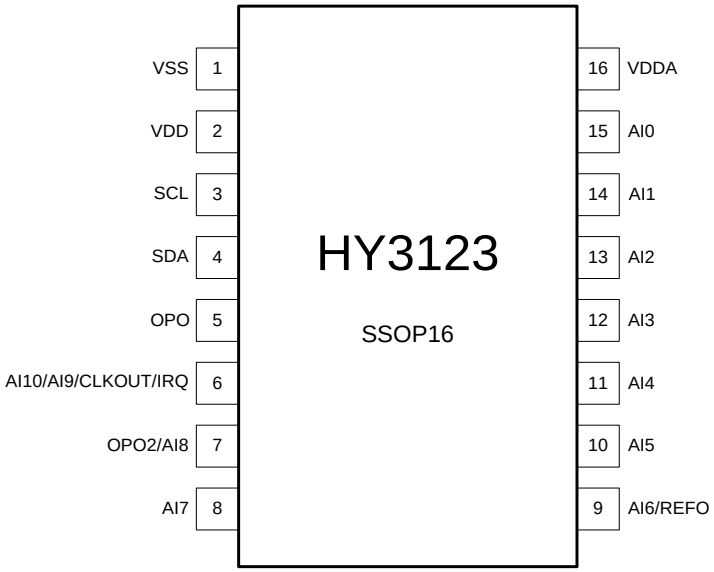


Figure 3-2 SSOP16 Pin Diagram

3.2. Pinout I/O Description

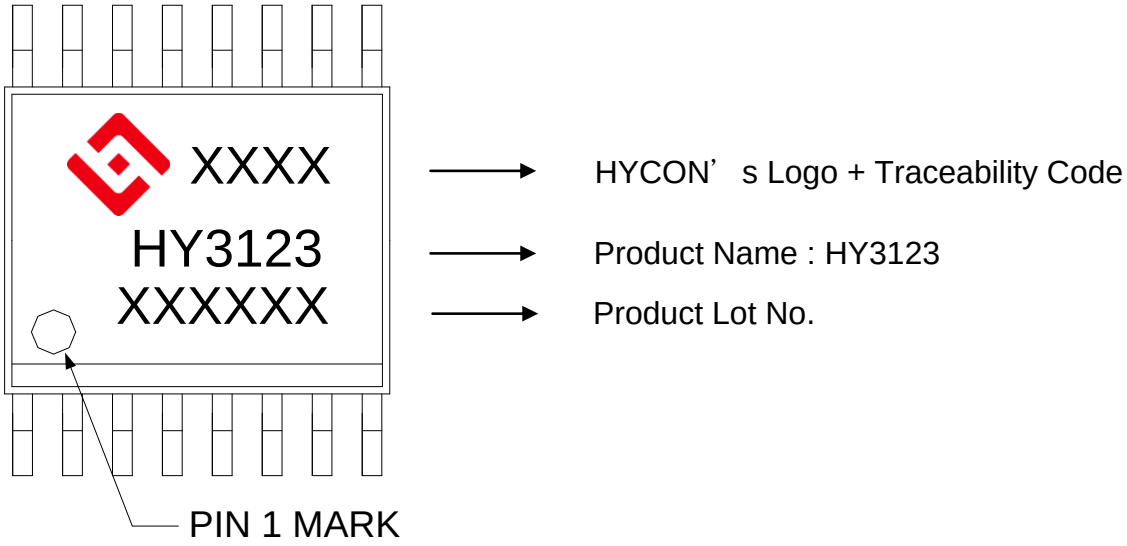
"I/O" Input/Output, "I" Input, "O" Output, "D" Digital Open-Drain, "S" Schmitt Trigger, "C" CMOS, "P" Power, "A" Analog

SSOP20	SSOP16	Pin Name	Characteristic		Description
			Type	Buffer	
1	1	VSS	P	P	Chip Power Ground.
2		NC	-	-	Not Connected, do not connect for proper operation
3	2	VDD	P	P	Chip Power Voltage Input, an external 1~10uF capacitor is required.
4	3	SCL	DIO	S	I²C communication interface clock pin.
5	4	SDA	DIO	S	I2C communication interface clock pin.
		IRQ*	DO	C	ADC Interrupt Status Output.(Multiplex Selection)
6	5	OPO	DAIO	A	OPAMP2 Output.
7	6	AI10	P	P	Analog Channel.
8	6	AI9	P	P	Analog Channel.
		CLKOUT	P	P	Internal RC frequency division output pin.
		IRQ	P	P	ADC Interrupt Status Output.
9	7	OPO2	DAIO	A	OPAMP3 Output.
10	7	AI8	AIO	A	Analog Channel.
11	8	AI7	AIO	A	Analog Channel.
12	9	AI6	AIO	A	Analog Channel.
		REFO	P	P	1.2V Reference Voltage Output, an external 0.1uF capacitor is required.
13	10	AI5	AIO	A	Analog Channel.
14	11	AI4	AIO	A	Analog Channel.
15	12	AI3	AIO	A	Analog Channel.
16	13	AI2	AIO	A	Analog Channel.
17	14	AI1	AIO	A	Analog Channel.
18	15	AI0	AIO	A	Analog Channel.
19		NC	-	-	Not Connected, do not connect for proper operation
20	16	VDDA	AIO	P	Regulator Output, analog circuit voltage source, an external 1~10uF capacitor is required. (source: VDD)

Table 3-1 Pin Definition and Function Description

3.3. Package Marking Information

3.3.1. SSOP package marking information



4. Application Circuit

4.1. HCT Glucose Meter Application

※ For detailed information on BIA Module, please contact the HYCON Technology contact window.

圖 4-1 HCT Glucose Meter Application

5. Register List

5.1. Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1

"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
001h	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	ENREFO	1000 0000	1000 0000	*,*,*,* *,*,*,*
002h	OSCCN1	DADC[1:0]		CLKOUT[1:0]		IRQMode[1:0]		IRQSEL	ENDAPU	0011 0000	00xx 0000	*,*,*,* *,*,*,*
003h	ADCH	ADC conversion high byte data register								0000 0000	0000 0000	r,r,r,r r,r,r,r
004h	ADCM	ADC conversion middle byte data register								0000 0000	0000 0000	r,r,r,r r,r,r,r
005h	ADCL	ADC conversion low byte data register							ADST	0000 0000	0000 0000	r,r,r,r r,r,r,r
00Fh	CHOPCN	DAFM	ENCH	ENINXCH			-	-	-	0000 0000	0000 0000	*,*,*,* *,*,*,*
010h	AD1CN1	ENAD1	OSRM	VREGN	OSR[3:0]				CMFR	0000 0000	0000 0000	*,*,*,* *,*,*,w1
011h	AD1CN2		ENACM	ENV12	VCMS	LDOPL	ADGN[2:0]			0000 0000	0000 0000	*,*,*,* *,*,*,*
012h	AD1CN3	VRH[1:0]		VRL[1:0]		DCSET[3:0]				0000 0000	0000 0000	*,*,*,* *,*,*,*
013h	AD1CN4	INP[3:0]				INN[3:0]				0000 0000	0000 0000	*,*,*,* *,*,*,*
014h	AD1CN5	-		ENTPS	TPSCH	INX[1:0]		-	-	0000 0000	0000 0000	*,*,*,* *,*,*,*
015h	DACCN1	ENAI10	DAPS[1:0]		DANS[1:0]		-	-	-	0000 0000	0000 0000	*,*,*,* *,*,*,*
016h	DACCN2	ENOP3	ENOP2	ENOP1	DADCS	DALH	-	-	ENDA	0000 0000	0000 0000	*,*,*,* *,*,*,*
017h	DACCN3	-	-	-	-	DABIT[11:8]				0000 0000	0000 0000	*,*,*,* *,*,*,*
018h	DACCN4	DABIT[7:0]								0000 0000	0000 0000	*,*,*,* *,*,*,*
019h	DAC2CN1	DAPS2[1:0]		DANS2[1:0]		DALH2	-	-	ENDA2	0000 0000	0000 0000	*,*,*,* *,*,*,*
01Ah	DAC2CN2	-	-	-	DADCS2	DABIT2[11:8]				0000 0000	0000 0000	*,*,*,* *,*,*,*
01Bh	DAC2CN3	DABIT2[7:0]								0000 0000	0000 0000	*,*,*,* *,*,*,*
01Ch	OP1NET1	-	-	OP1OS[5:3]			-	-	-	0000 0000	0000 0000	*,*,*,* *,*,*,*
01Dh	OP1NET2	OP1PS[7:1]							-	0000 0000	0000 0000	*,*,*,* *,*,*,*
01Eh	OP1NET3	OP1NS[7:0]								0000 0000	0000 0000	*,*,*,* *,*,*,*
01Fh	OP2NET1	-	-	-	-	-	-	OP2NS[9:8]		0000 0000	0000 0000	*,*,*,* *,*,*,*
020h	OP2NET2	OP2NS[7:0]								0000 0000	0000 0000	*,*,*,* *,*,*,*
021h	OP2NET3	OP2PS[7:0]								0000 0000	0000 0000	*,*,*,* *,*,*,*
022h	OP3NET1	S4	-	S2	-	-	-	-	-	0000 0000	0000 0000	*,*,*,* *,*,*,*
023h	OP3NET2	OP3NS[7:0]								0000 0000	0000 0000	*,*,*,* *,*,*,*
024h	OP3NET3	OP3PS[7:0]								0000 0000	0000 0000	*,*,*,* *,*,*,*
02Bh	HAOTRIM	-	HAOTR[6:0]							0100 0000	uuuu uuuu	*,*,*,* *,*,*,*
03Eh	HAOCTL	ENHAO	HAOM1	HAOM0	-	-	-	-	TRIMON	0000 0u00	0000 0x00	*,*,*,* *,*,*,*

Table 5-1 Register List

5.2. Register Description

5.2.1. PWRCN Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
001h	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	ENREFO	1000 0000	1000 0000	*,*,*,* *,*,*,*

Table 5-2 PWRCN Control Register

PWRCN Control Register:

Bit	Name	Description
Bit7	ENBGR	Internal Bandgap Reference Voltage Controller. <0> Disable. When turned off, the internal HAO frequency will turns off and the chip will enter Sleep mode. <1> Enable(default), ENBGR must be set to '1' before turning on the ADC and TPS.
Bit6~4	LDOC[2:0]	VDDAX Output Voltage Selector When ENLDO is '1', this setting voltage is output to the VDDA pin. LDOC[2:0] / VDDAX Output Voltage / LDOC[2:0] / VDDAX Output Voltage 000 / 2.4V / 100 / 3.6V 001 / 2.6V / 101 / 2.3V 010 / 2.9V / 110 / 2.25V 011 / 3.3V / 111 / 2.2V Note: In practical applications, VDDA must be less than VDD-0.25V.
Bit3~2	LDOM[1:0]	VDDA Output Selector When ENLDO is '0', this setting is output to the VDDA pin. <00> Disable(default), VDDA will be high input impedance mode <01> Output VDD Voltage <10> Pull high to VDD by 1.5mA. (It is use to initial VDDA when a small current) <11> Reserved.
Bit1	ENLDO	Internal VDDA Linear Regulator Controller <0> Disable(default) <1> Enable
Bit1	ENREFO	REFO Reference voltage source output control <0> Disable(default), VDDA will be high input impedance mode <1> 1.2V Voltage source output

5.2.2. OSCCN1 Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
002h	OSCCN1	DADC[1:0]		CLKOUT[1:0]		IRQMode[1:0]		IRQSEL	ENDAPU	0011 0000	00xx 0000	*,*,*,* *,*,*,*

Table 5-3 OSCCN1 Control Register

OSCCN1 Control Register:

Bit	Name	Description
Bit7~6	DADC[2:0]	ADC Clock Frequency Divider Selector <00> Pre-Scale: HAO ÷ 4(default) <01> Pre-Scale: HAO ÷ 8 <10> Pre-Scale: HAO ÷ 2 <11> Reserved
Bit5~4	CLKOUT[1:0]	CLKOUT Function Output Selector. (output pin is CLKOUT) <00> Disable output, it is a high impedance input state <01> Internal HAO Frequency output, Pre-Scale: HAO ÷ 512 <10> Internal HAO Frequency output, Pre-Scale: HAO ÷ 4096

Bit	Name	Description
		<11> Input VSS potential.(default)
Bit3~2	IRQMode[1:0]	IRQ Function Output Selector. <00> Disable the IRQ output function <01> Enable IRQ mdoe, IRQ pin output low-level: When ADC interrupt, the IRQ pin is output to the Low Level. 1. When IRQSEL<0>=CLKOUT, The IRQ will not release the state and return to High Level until the behavior of the Host Read Register (including ADCH~ADQL, 03H~0BH) occurs. The setting priority is higher than the CLKOUT[1:0] setting, when IRQMode[1:0] =01b or 10b is set, the setting of CLKOUT[1:0] will be invalid. 2. When IRQSEL<0>= SDA, When the ADC conversion is completed and the IRQ interrupt needs to be triggered, if the I²C communication is in progress, the SDA output Low Level will occur after the I²C Stop. After that, you need to send Low Pulse through SCL to unlock SDA, and then you can re-run I²C communication. <10> Enable IRQ mdoe, IRQ pin output low pulse: When the ADC is interrupted, the IRQ pin output low pulse is maintained for 16 ADC Clock times (ADC Clock=1MHz, Low Pulse Time=1M/16=16 uS). 1. When IRQSEL<0>=CLKOUT, When the ADC is interrupted, the IRQ pin outputs low pulse normally. The setting priority is higher than the CLKOUT[1:0] setting, when IRQ Mode[1:0] =01b or 10b is set, the setting of CLKOUT[1:0] will be invalid. 2. When IRQSEL<0>=SDA, When the ADC conversion is completed and the IRQ interrupt needs to be triggered, if the I²C communication is in progress, the SDA output Low Pulse will occur after the I²C Stop. Host needs to correctly set the Host GPIO with High to Low trigger function before waiting for IRQ Low Pulse to avoid data leakage.
Bit1	IRQSEL	IRQ Function Output Pin Selector <0> CLKOUT(default) <1> As SDA pin IRQ Mode startup and setting, determined by IRQMode[1:0]
Bit0	ENDAPU	AI9 Pin Pull-up Resistor Selector <0> Disable the pull-up register(default) <1> Enable 400K ohm pull-up resistor to VDDA pin

5.2.3. ADCH ~ ADCL Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
003h	ADCH	ADC conversion high byte data register								0000 0000	0000 0000	r,r,r,r r,r,r,r
004h	ADCM	ADC conversion middle byte data register								0000 0000	0000 0000	r,r,r,r r,r,r,r
005h	ADCL	ADC conversion low byte data register							ADST	0000 0000	0000 0000	r,r,r,r r,r,r,r

Table 5-4 ADCH ~ ADCL Data Register

ADCH[7:0]、ADCM[7:0]、ADCL[7:0] ADC Data Conversion Register:

Bit	Name	Description
Bit7~0	ADCH[7:0]	ADC High Byte Data Register
Bit7~0	ADCM[7:0]	ADC Middle Byte Data Register
Bit7~1	ADCL[7:1]	ADC Low Byte Data Register
Bit0	ADST	ADC Data Reading Flag <0> ADC data has been read or ADC interrupt event has not occurred <1> ADC has updated the data and an interrupt flag has occurred. When the bit is read, the hardware will automatically clear the bit to 0

The ADCH register supports the I²C continuous read data function. When the I²C communication needs to read the ADCH~ADCL register, the 24-bit ADC data conversion value can be directly read by the Host through the continuous reading mode. When the ADCH~ADCL register is re-read when the next ADC interrupt occurs,

the Host can directly read the data without re-pointing the Point Address. The read protocol can be described with reference to Figure 7-11.

5.2.4. CHOPCN Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
00Fh	CHOPCN	DAFM	ENCH	ENINXCH						0000 0000	0000 0000	*,*,*,*,*,*,*,*

Table 5-6 CHOPCN Control Register

CHOPCN Control Register:

Bit	Name	Description
Bit7	DAFM	Comb Filter Output Data Format. <0> Normal data output(default) <1> Chopper result data output (ADC1 + (ADC2))/2, the next one is: (ADC2 + ADC3)/2.... and so on
Bit6	ENCH	ADC Chopper Mode Controller <0> Disable(default) <1> Enable Note: Must first set ENINXCH and DAFM, and finally turn on ENCH.
Bit5	ENINXCH	Control ADC Input INX[1:0] Automatic Switch <0> Disable(default), INX maintains the original user settings <1> Enable automatic switch

5.2.5. AD1CN1 ~ AD1CN5 Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
010h	AD1CN1	ENAD1	OSRM	VREGN	OSR[3:0]				CMFR	0000 0000	0000 0000	*,*,*,*,*,*,*,w1
011h	AD1CN2		ENACM	ENV12	VCMS	LDOPL	ADGN[2:0]			0000 0000	0000 0000	*,*,*,*,*,*,*,*
012h	AD1CN3	VRH[1:0]		VRL[1:0]		DCSET[3:0]				0000 0000	0000 0000	*,*,*,*,*,*,*,*
013h	AD1CN4	INP[3:0]				INN[3:0]				0000 0000	0000 0000	*,*,*,*,*,*,*,*
014h	AD1CN5	-		ENTPS	TPSCH	INX[1:0]				0000 0000	0000 0000	*,*,*,*,*,*,*,*

Table 5-7 AD1CN1 ~ AD1CN5 Control Register

AD1CN1 Control Register:

Bit	Name	Description
Bit7	ENAD1	ΣΔADC Enable Controller <0> Disable(default) <1> Enable
Bit6	OSRM	Comb Filter Level <0> 2nd comb filter(default) <1> 3rd comb filter
Bit5	VREGN	ADC Voltage Reference VR± Gain Setting <0> x1(default) <1> x1/2
Bit4~1	OSR[3:0]	ΣΔADC Oversampling rate divider
Bit0	CMFR	ΣΔADC and Comb Filter Reset Controller.

OSR[3:0]	OSR	Comb filter Order	OSR[3:0]	OSR	Comb filter Order
0000	32	2nd/3rd	1000	8000	2nd/3rd
0001	64	2nd/3rd	1001	16000	2nd/3rd
0010	125	2nd/3rd	1010	32000	2nd/3rd
0011	250	2nd/3rd	1011	64000	2nd/3rd
0100	500	2nd/3rd	1100	64000	2nd/3rd
0101	1000	2nd/3rd	1101	64000	2nd/3rd
0110	2000	2nd/3rd	1110	64000	2nd/3rd
0111	4000	2nd/3rd	1111	64000	2nd/3rd

		<0> Not reset <1> Reset occurs when CMFR is set to 1, this bit is write 1 only and the hardware is automatically cleared to 0.

AD1CN2 Control Register:

Bit	Name	Description
Bit6	ENACM	ADC Common Mode Buffer Enable Controller <0> Disable(default) <1> Enable, the voltage is determined according to VCMS.
Bit5	ENV12	V12_1 Voltage Source Controller <0> Select REFO as the source of V12_1(default) <1> Select V12 as the source of V12_1
Bit4	VCMS	ADC Common Voltage. <0> VDDA/2(default) <1> 1.2V
Bit3	LDOPL	Internal 250kΩ pull-down Resistor Switch <0> Disable(default) <1> Enable The LDOPL must be set to 1 in the following cases, otherwise the VDDA voltage regulation result will be worse than expected. ※ When using internal LDO output. (ENLDO=1b) ※ When the ADC reference voltage is VDDA/2-VSS. (VCMS=0b)
Bit2~0	ADGN[2:0]	ADC Input Gain Setting

ADGN[2:0]	Gain	ADGN[2:0]	Gain
000	x1/4	100	x4
001	x1/2	101	x8
010	x1	110	x16
011	x2	111	x16

AD1CN3 Control Register:

Bit	Name	Description
Bit7~6	VRH[1:0]	ADC Reference Voltage Positive Input Selection Control <00> VDDA(default) <01> AI6 <10> AI9 <11> V12_1
Bit5~4	VRL[1:0]	ADC Reference Voltage Negative Input Selection Control <00> VSSA(default) <01> AI5 <10> AI6 <11> V12_1
Bit3~0	DCSET[3:0]	SI± Bias Voltage Adjuster

DCSET<3:0>	Offset	DCSET<3:0>	Offset
0000	0	1000	0
0001	+1/8*(REFP–REFN)	1001	-1/8*(REFP–REFN)
0010	+2/8*(REFP–REFN)	1010	-2/8*(REFP–REFN)
0011	+3/8*(REFP–REFN)	1011	-3/8*(REFP–REFN)
0100	+4/8*(REFP–REFN)	1100	-4/8*(REFP–REFN)
0101	+5/8*(REFP–REFN)	1101	-5/8*(REFP–REFN)
0110	+6/8*(REFP–REFN)	1110	-6/8*(REFP–REFN)
0111	+7/8*(REFP–REFN)	1111	-7/8*(REFP–REFN)

AD1CN4 Control Register:

Bit	Name	Description
Bit7~4	INP[3:0]	ADC Positive Input Signal Selector
Bit3~0	INN[3:0]	ADC Negative Input Signal Selector

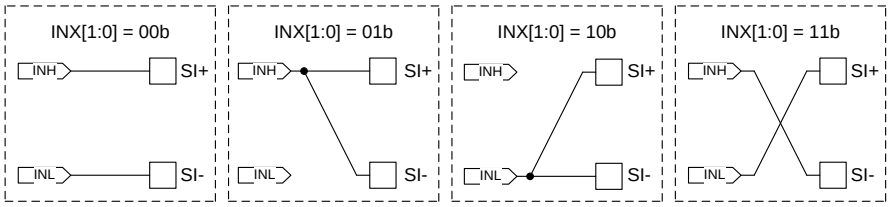
ADC Positive Input Signal Selector

INP<3:0>	ADC Input Channel	INP<3:0>	ADC Input Channel
0000	VSSA	1000	AI0
0001	OP2O	1001	AI2
0010	TS0	1010	AI4
0011	TS1	1011	AI6
0100	VDD/10	1100	AI8
0101	V12_1	1101	AI9
0110	VDDA	1110	OP3O
0111	OPO	1111	OPO2

ADC Negative Input Signal Selector

INN<3:0>	ADC Input Channel	INN<3:0>	ADC Input Channel
0000	VSSA	1000	OPO
0001	OP1O	1001	AI1
0010	TS0	1010	AI3
0011	TS1	1011	AI5
0100	DACO	1100	AI6
0101	V12_1	1101	AI7
0110	-	1110	AI10
0111	-	1111	R_N

AD1CN5 Control Register:

Bit	Name	Description
Bit5	ENTPS	Internal TPS Enable Control <0> Disable(default) <1> Enable, need to set the relative ADC network
Bit4	TPSCH	TPS Output Reverse Control <0> Forward(default) <1> Reverse
Bit3~2	INX	SI± Input Signal Transposer <00> INH→SI+,INL→SI-(default) <01> INH→SI+,INH→SI- & INL floating <10> INL→SI+,INL→SI- & INH floating <11> INL→SI+,INH→SI- The INX[1:0] setting status is as illustrated below. 

5.2.6. DACCN1 ~ DACCN4 Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
015h	DACCN1	ENAI10	DAPS[1:0]		DANS[1:0]		-	-	-	0000 0000	0000 0000	*,*,*,*,*,*,*,*
016h	DACCN2	ENOP3	ENOP2	ENOP1	DADCS	DALH	-	-	ENDA	0000 0000	0000 0000	*,*,*,*,*,*,*,*
017h	DACCN3	-	-	-	-	DABIT[11:8]				0000 0000	0000 0000	*,*,*,*,*,*,*,*
018h	DACCN4	DABIT[7:0]								0000 0000	0000 0000	*,*,*,*,*,*,*,*

Table 5-8 DACCN1 ~ DACCN4 Control Register

DACCN1 Control Register:

Bit	Name	Description

Bit	Name	Description
Bit7	ENAI10	AI10 PAD Switch Selection <0> OFF(default), AI10 switch is off, AI10 is HiZ state, no input function <1> AI10 ON
Bit6~5	DAPS[1:0]	12-bit Resistance Ladder Ⅰ Positive Input Source Selection <00> VDDA(default) <01> AI0 <10> AI2 <11> AI6
Bit4~3	DANS[1:0]	12-bit Resistance Ladder Ⅰ Negative Input Source Selection <00> VSSA(default) <01> AI0 <10> AI6 <11> AI9

DACCN2 Control Register:

Bit	Name	Description
Bit7	ENOP3	Rail to Rail OPAMP3 Enable Controller <0> Disable(default) <1> Enable
Bit6	ENOP2	Rail to Rail OPAMP2 Enable Controller <0> Disable(default) <1> Enable
Bit5	ENOP1	Rail to Rail OPAMP1 Enable Controller <0> Disable(default) <1> Enable
Bit4	DADCS	12-bit Resistance Ladder Ⅰ Compensation Controller <0> No compensation(default) <1> Compensation
Bit3	DALH	12-bit Resistance Ladder Ⅰ Control Output to DACO <0> Disable(default) <1> Enable
Bit0	ENDA	12-bit Resistance Ladder Ⅰ Function Enable Control <0> Disable(default) <1> Enable

DACCN3 Control Register:

Bit	Name	Description
Bit3~0	DABIT[11:8]	12-bit resistance ladder Ⅰ Bit11~ Bit8 Ratio setting of Output Voltage

DACCN4 Control Register:

Bit	Name	Description
Bit7~0	DABIT[7:0]	12-bit resistance ladder Ⅰ Bit7~ Bit0 Ratio setting of Output Voltage

5.2.7. DAC2CN1 ~ DAC2CN3 Register

“.”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
019h	DAC2CN1	DAPS2[1:0]		DANS2[1:0]		DALH2	-	-	ENDA2	0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Ah	DAC2CN2	-	-	-	DADCS2	DABIT2[11:8]				0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Bh	DAC2CN3	DABIT2[7:0]								0000 0000	0000 0000	*,*,*,*,*,*,*,*

Table 5-9 DAC2CN1 ~ DAC2CN3 Control Register

DAC2CN1 Control Register:

Bit	Name	Description
Bit7~6	DAPS2[1:0]	12-bit Resistance Ladder Ⅱ Positive Input Source Selection <00> VDDA(default) <01> AI0 <10> AI10 <11> AI6

Bit	Name	Description
Bit5~4	DANS2[1:0]	12-bit Resistance Ladder **II** Negative Input Source Selection <00> VSSA(default) <01> AI0 <10> AI6 <11> AI9
Bit3	DALH2	12-bit Resistance Ladder **II** Control Output to DACO2 <0> Disable(default) <1> Enable
Bit0	ENDA2	12-bit Resistance Ladder **II** Function Enable Control <0> Disable(default) <1> Enable

DAC2CN2 Control Register:

Bit	Name	Description
Bit4	DADCS2	12-bit Resistance Ladder **II** Compensation Controller <0> No compensation(default) <1> Compensation
Bit3~0	DABIT2[11:8]	12-bit Resistance Ladder **II** Bit11~ Bit8 Ratio setting of Output Voltage

DAC2CN3 Control Register:

Bit	Name	Description
Bit7~0	DABIT2[7:0]	12-bit Resistance Ladder II Bit7~ Bit0 Ratio setting of Output Voltage

5.2.8. OP1NET1 ~ OP1NET3 Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
01Ch	OP1NET1	-	-	OP1OS[5:3]			-	-	-	0000 0000	0000 0000	*,*,*,* *,*,*,*
01Dh	OP1NET2	OP1PS[7:1]							-	0000 0000	0000 0000	*,*,*,* *,*,*,*
01Eh	OP1NET3	OP1NS[7:0]								0000 0000	0000 0000	*,*,*,* *,*,*,*

Table 5-10 OP1NET1 ~ OP1NET3 Control Register

OP1NET1[7:0] Rail to Rail OPAMP1 Output Switch Control Register:

Bit	Name	Description
Bit5	OP1OS[5]	<0> Off(default) <1> AI8
Bit4	OP1OS[4]	<0> Off(default) <1> AI6
Bit3	OP1OS[3]	<0> Off(default) <1> AI4

OP1NET2[7:0] Rail to Rail OPAMP1 Positive Input Switch Control Register:

Bit	Name	Description
Bit7	OP1PS[7]	<0> Off(default) <1> AI7
Bit6	OP1PS[6]	<0> Off(default) <1> AI6
Bit5	OP1PS[5]	<0> Off(default) <1> AI5
Bit4	OP1PS[4]	<0> Off(default) <1> AI3
Bit3	OP1PS[3]	<0> Off(default) <1> AI1
Bit2	OP1PS[2]	<0> Off(default) <1> V12
Bit1	OP1PS[1]	<0> Off(default) <1> DACO

OP1NET3[7:0] Rail to Rail OPAMP1 Negative Input Switch Control Register:

Bit	Name	Description
Bit7	OP1NS[7]	<0> Off(default) <1> AI9
Bit6	OP1NS[6]	<0> Off(default) <1> AI8
Bit5	OP1NS[5]	<0> Off(default) <1> AI7
Bit4	OP1NS[4]	<0> Off(default) <1> AI5
Bit3	OP1NS[3]	<0> Off(default) <1> AI3
Bit2	OP1NS[2]	<0> Off(default) <1> AI1
Bit1	OP1NS[1]	<0> Off(default) <1> DACO
Bit0	OP1NS[0]	<0> Off(default) <1> OP1O

5.2.9. OP2NET1 ~ OP2NET3 Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
01Fh	OP2NET1	-	-	-	-	-	-	OP2NS[9:8]		0000 0000	0000 0000	*,*,*,*,*,*,*,*
020h	OP2NET2	OP2NS[7:0]								0000 0000	0000 0000	*,*,*,*,*,*,*,*
021h	OP2NET3	OP2PS[7:0]								0000 0000	0000 0000	*,*,*,*,*,*,*,*

Table 5-11 OP2NET1 ~ OP2NET3 Control Register

OP2NET1[7:0] Rail to Rail OPAMP2 Control Register:

Bit	Name	Description
Bit1	OP2NS[9]	<0> Off(default) <1> OPO
Bit0	OP2NS[8]	<0> Off(default) <1> AI9

OP2NET2[7:0] Rail to Rail OPAMP2 Negative Input Switch Control Register:

Bit	Name	Description
Bit7	OP2NS[7]	<0> Off(default) <1> AI7
Bit6	OP2NS[6]	<0> Off(default) <1> AI6
Bit5	OP2NS[5]	<0> Off(default) <1> AI5
Bit4	OP2NS[4]	<0> Off(default) <1> AI3
Bit3	OP2NS[3]	<0> Off(default) <1> AI1
Bit2	OP2NS[2]	<0> Off(default) <1> DACO2
Bit1	OP2NS[1]	<0> Off(default) <1> OP2O
Bit0	OP2NS[0]	<0> Off(default) <1> OP1O

OP2NET3[7:0] Rail to Rail OPAMP2 Positive Input Switch Control Register:

Bit	Name	Description
Bit7	OP2PS[7]	<0> Off(default)

		<1> AI7
Bit6	OP2PS[6]	<0> Off(default) <1> AI6
Bit5	OP2PS[5]	<0> Off(default) <1> AI5
Bit4	OP2PS[4]	<0> Off(default) <1> AI3
Bit3	OP2PS[3]	<0> Off(default) <1> AI1
Bit2	OP2PS[2]	<0> Off(default) <1> V12
Bit1	OP2PS[1]	<0> Off(default) <1> OP1O
Bit0	OP2PS[0]	<0> Off(default) <1> DACO2

5.2.10. OP3NET1 ~ OP3NET3 Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
022h	OP3NET1	S4	S3	S2	S1	Rfb2[1:0]		-	-	0000 0000	0000 0000	*,*,*,*,*,*,*,*
023h	OP3NS	OP3NS[7:0]								0000 0000	0000 0000	*,*,*,*,*,*,*,*
024h	OP3PS	OP3PS[7:0]								0000 0000	0000 0000	*,*,*,*,*,*,*,*

Table 5-12 OP3NET1 ~ OP3NET3 Control Register

OP3NET1[7:0] Rail to Rail OPAMP3 Control Register:

Bit	Name	Description
Bit7	S4	Connection Switch Control between OP3O and OPO2 PAD <0> Open(default) <1> Close, the OPAMP3 output OP3O shorted to OPO2 PAD
Bit5	S2	Connection Switch Control between OP2O and OPO PAD <0> Open(default) <1> Close, the OPAMP2 output OP2O shorted to OPO PAD

OP3NET2[7:0] Rail to Rail OPAMP3 Negative Input Switch Control Register:

Bit	Name	Description
Bit7	OP3NS[7]	<0> Off(default) <1> OPO2
Bit6	OP3NS[6]	<0> Off(default) <1> AI10
Bit5	OP3NS[5]	<0> Off(default) <1> AI9
Bit4	OP3NS[4]	<0> Off(default) <1> AI7
Bit3	OP3NS[3]	<0> Off(default) <1> AI6
Bit2	OP3NS[2]	<0> Off(default) <1> AI5
Bit1	OP3NS[1]	<0> Off(default) <1> DACO2
Bit0	OP3NS[0]	<0> Off(default) <1> OP3O

OP3NET3[7:0] Rail to Rail OPAMP3 Positive Input Switch Control Register:

Bit	Name	Description
Bit7	OP3PS[7]	<0> Off(default)

		<1> DACO
Bit6	OP3PS[6]	<0> Off(default) <1> AI10
Bit5	OP3PS[5]	<0> Off(default) <1> AI6
Bit4	OP3PS[4]	<0> Off(default) <1> AI3
Bit3	OP3PS[3]	<0> Off(default) <1> AI1
Bit2	OP3PS[2]	<0> Off(default) <1> V12
Bit1	OP3PS[1]	<0> Off(default) <1> OP1O
Bit0	OP3PS[0]	<0> Off(default) <1> DACO2

5.2.11. HAOTRIM Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
02Bh	HAOTRIM	-	HAOTR[6:0]							0100 0000	uuuu uuuu	*,*,*,*,*,*,*,*

Table 5-14 HAOTRIM Control Register

HAOTRIM[7:0] HAO Frequency Adjustment Control Register:

Bit	Name	Description
Bit6~0	HAOTR[6:0]	HAO Frequency Center Adjustment Controller <0000000> Adjustable Upper Limit . <1000000> Center point 0.0% . <1111111> Adjustable Lower Limit Trim LSB ~ 0.5%

5.2.12. HAOCTL Register

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IIC RST	R/W
03Dh	TST	RSV.								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
03Eh	HAOCTL	ENHAO	HAOM1	HAOM0	-	-	-	-	TRIMON	1000 0u00	1000 0x00	*,*,*,*,*,*,*,*

Table 5-15 HAOCTL Control Register

TST[7:0] Reserved Byte:

Bit	Name	Description
Bit7~0	TST[7:0]	Reserved, do not change the value, the default value is 0x00

HAOCTL[7:0] Frequency Controller Controls Register:

Bit	Name	Description
Bit7	ENHAO	HAO Enable Control Bit <0> Enable internal high speed HAO oscillator(default) <1> Disable internal high speed HAO oscillator
Bit6~5	HAOM[1:0]	HAO Frequency Control Bit <00> 2MHz HAO(default) <01> 4MHz HAO <10> 8MHz HAO <11> Reserved
Bit0	TRIMON	HAO Trim Value Write Protection Control Bit <0> Unprotected status(default), you can update the HAOTRIM :HAOTR[6:0]

		value. <1> Protection status, you can not update the HAOTRIM :HAOTR[6:0] value.

6. Elctrical Characteristic

6.1. ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)
Voltage applied at VDD to VSS . . . . . −0.2 V to 6.0 V
Voltage applied to any pin . . . . . −0.2 V to VDD + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature . . . . . −55℃ to 150℃
Operation temperature . . . . . −40℃ to 85℃
Total power dissipation. 0.5w
Maximum output current sink by CLKOUT pin 20mA

6.2. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	All digital peripherals	2.2		5.5	V
V_{DDA}	Supply Voltage	Analog peripherals	2.2		4.5	
V_{SS}	Supply Voltage		0		0	

6.3. Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator frequency	2MHz Mode, HAOM[1:0]=00b	1.65	1.95	2.25	MHz
		4MHz Mode, HAOM[1:0]=01b	3.45	4.0	4.56	MHz
		8MHz Mode, HAOM[1:0]=10b	7.57	8.5	9.16	MHz
		HAO Trim Range[6:0]	-63		64	LSB
		2MHz HAO Trim LSB		0.345		%
		4MHz HAO Trim LSB		0.3		%
		8MHz HAO Trim LSB		0.21		%

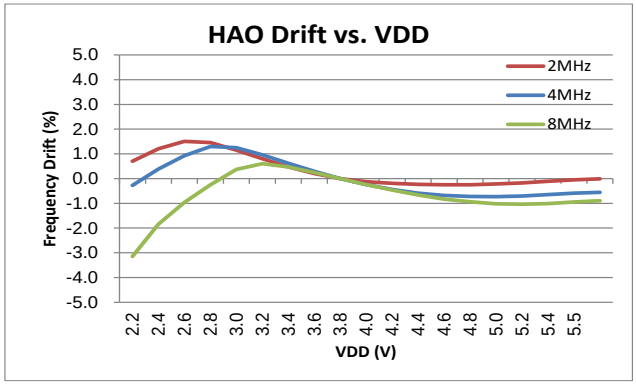


Figure 6.3-1 HAO vs. VDD

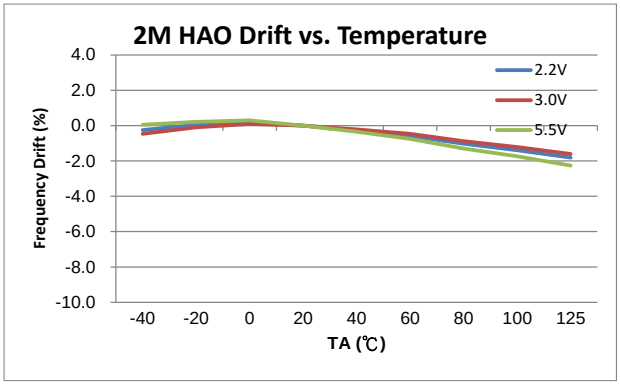


Figure 6.3-2 HAO(2.0MHz) vs. Temperature

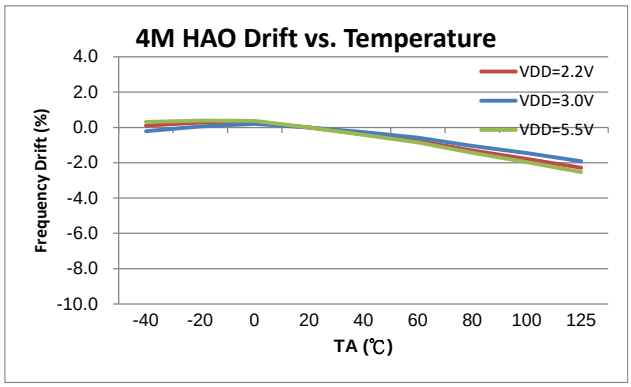


Figure 6.3-3 HAO(4.0MHz) vs. Temperature

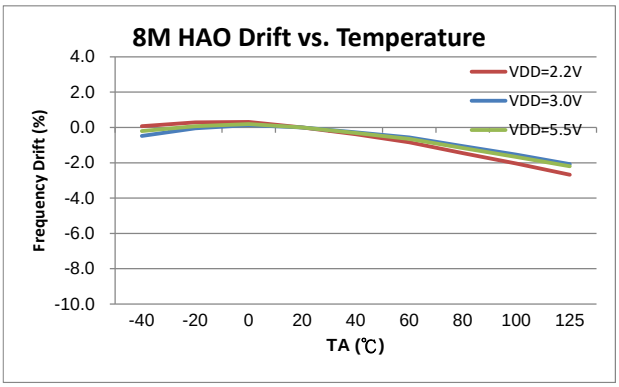


Figure 6.3-4 HAO(8.0MHz) vs. Temperature

6.4. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LP3}	Low Power 3	HAO = off, All IP Off, Sleep state		0.3	1.0	uA
HAO：Internal High Accuracy Oscillator frequency.						

T_A = 25℃,V_{DD} = 5.5V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LP3}	Low Power 3	HAO = off, All IP Off, Sleep state		0.5	2	uA

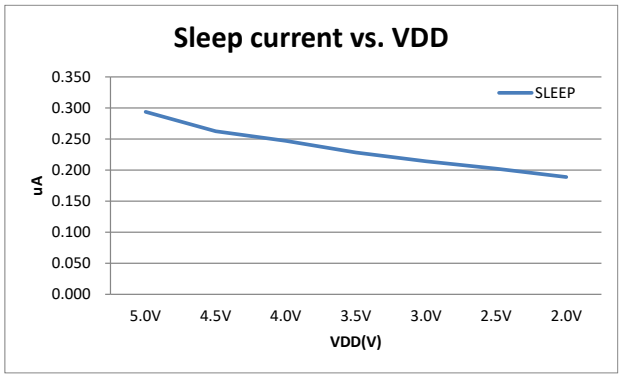


Figure 6.4-1 I_{LP3} vs. VDD

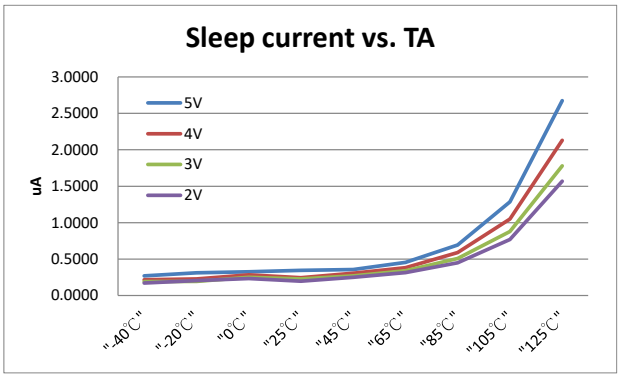


Figure 6.4-2 I_{LP3} vs. Temperature

6.5. GPIO PORT CLKOUT/IRQ/AI9

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Analog Input						
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance		351	390	429	kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD<4V, I_{OH}=10mA,	V_{DD} -0.3			V
		VDD>=4V, I_{OH}=15mA,	V_{DD} -0.4			
V_{OL}	Low-level output voltage	VDD<4V, I_{OL}=-10mA			V_{SS} +0.3	
		VDD>=4V, I_{OL}=-15mA			V_{SS} +0.4	

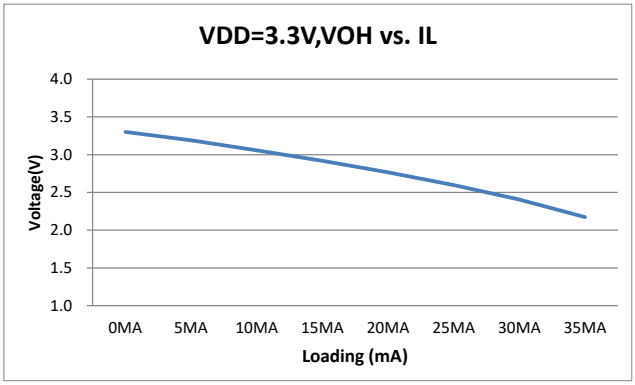


Figure 6.5-1 V_{OH} vs. I_{OH}

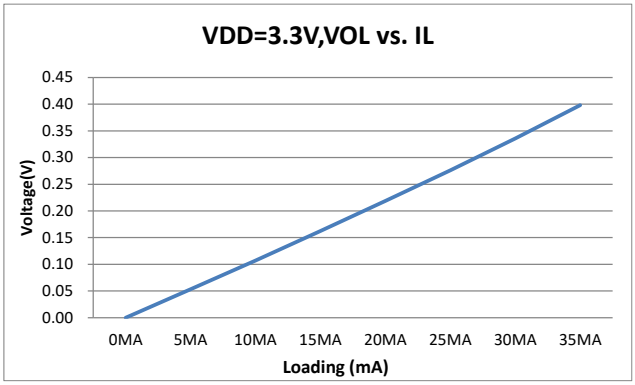


Figure 6.5-2 V_{OL} vs. I_{OL}

6.6. Brownout Reset (BOR)

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BOR	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR}$		2			uS
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}	T_A = 25℃	1.5	1.65	1.8	V
	V_{DD} Start Voltage to accepted reset internally (L➔H),$V_{LVR,}$	T_A = -40℃ ~ 85 ℃	1.45		1.85	V
	Current consumption	VDD=3.3V		0.3		uA
		VDD=5.5V		0.5		uA

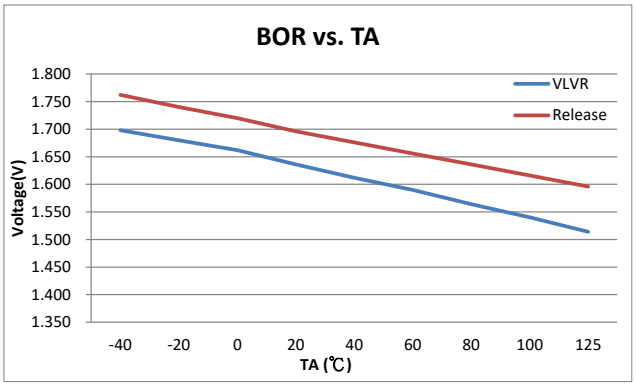


Figure 6.6-1 BOR vs. Temperature

6.7. Power System

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧ VDDA+0.25V	LDOC [2:0]=000b	2.28	2.4	2.52	V
			LDOC [2:0]=001b	2.47	2.6	2.73	V
			LDOC [2:0]=010b	2.755	2.9	3.045	V
			LDOC [2:0]=011b	3.135	3.3	3.465	V
			LDOC [2:0]=100b	3.42	3.6	3.78	V
			LDOC [2:0]=101b	2.19	2.3	2.42	V
			LDOC [2:0]=110b	2.14	2.25	2.36	V
			LDOC [2:0]=111b	2.09	2.2	2.31	V
	Dropout voltage	I_L = 10mA	LDOC [2:0]=000b		400		mV
	Temperature drift	LDOC [2:0]=000b I_L = 10uA	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	LDOC [2:0]=000b	V_{DD}=VDDA+0.25V~5.5V		±0.2		%/V
REFO	REFO operation current, I_{REFO}	VDDA=2.4V, ENV12=1b			50		uA
	output voltage, V_{REFO}		I_L = 0mA,	1.14	1.2	1.26	V
			I_L = 0.2mA (include ESD resistance)	0.94		0.96	V_{REFO}
	Temperature drift		T_A=-40℃~85℃		50		ppm/℃
	V_{DDA} Voltage drift				100		uV/V
ACM	ACM operation current, I_{ACM}	VDDA=2.4V, ENADC[0]=1b, ENACM=1b			50		uA
	Internal Analog Common Mode Voltage ,V_{ACM}=1.2V or V_{ACM} VDDA/2		VCMS=0b, I_L = 0uA		VDDA/2		V
			VCMS=1b, I_L = 0uA	1.14	1.2	1.26	V
	Temperature drift		T_A=-40℃~85℃, ENACM [0]=1b		50		ppm/℃
VDDA：Adjust Voltage Regulator, ACM：Internal Analog Common Mode Voltage VDDA/2 (No voltage output) or 1.2V							

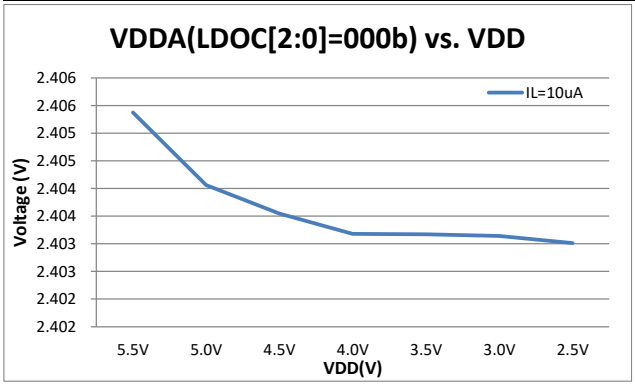


Figure 6.7-1 VDDA(000b) vs. VDD

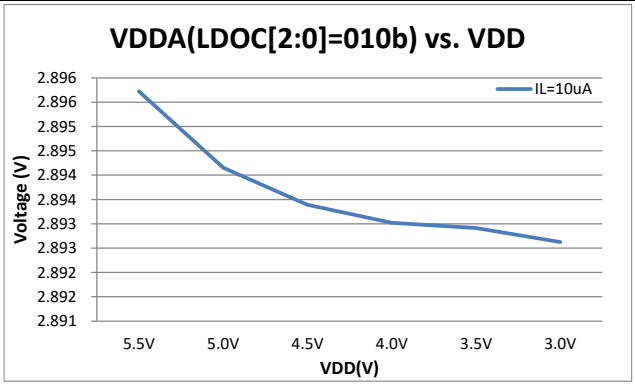


Figure 6.7-2 VDDA(010b) vs. VDD

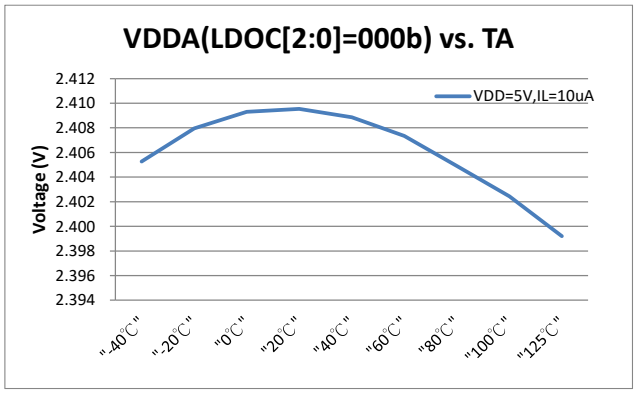


Figure 6.7-3 VDDA(000b) vs. Temperature

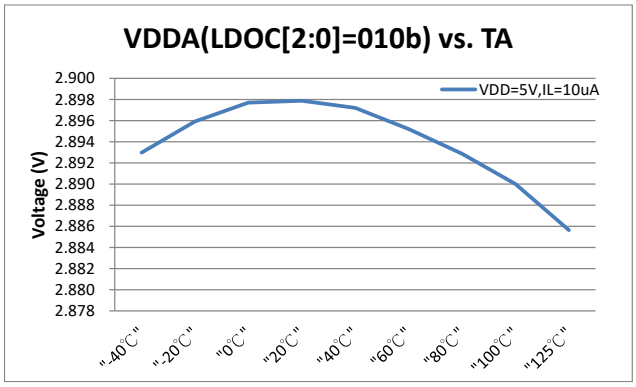


Figure 6.7-4 VDDA(000b) vs. Temperature

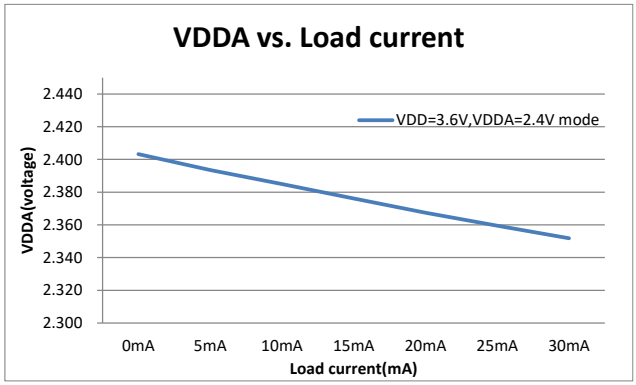


Figure 6.7-5 VDDA vs. Load current

6.8. ΣΔADC, Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.2		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK				1000		KHz
	Over Sample Ratio, OSR			64		65536	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1	GAIN =16, ADC_CK=1MHz		260		uA

6.8.1. ΣΔADC, performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,V_{VR}=1.0V,GAIN=1 without PGA,fSD18=1MHz,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV			±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV					
	No Missing Codes[3]	ADC_CK=1MHz,OSR=64000		23			Bits
G_{SD18}	Temperature drift Gain x16	T_A = -40℃~ 85℃,			10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper	ΔAI=0V ΔVR=1.2V DCSET[3:0]=<0000> *ΔAI is external short	Gain=2			1	%FSR
	Offset error temperature drift with chopper		GAIN=1		0.004		uV/℃
			GAIN=2		0.003		
			GAIN=4		0.003		
			GAIN=16		0.002		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V	V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V	V_{SI}=0V, GAIN=16		75		
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100 mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off		75		dB

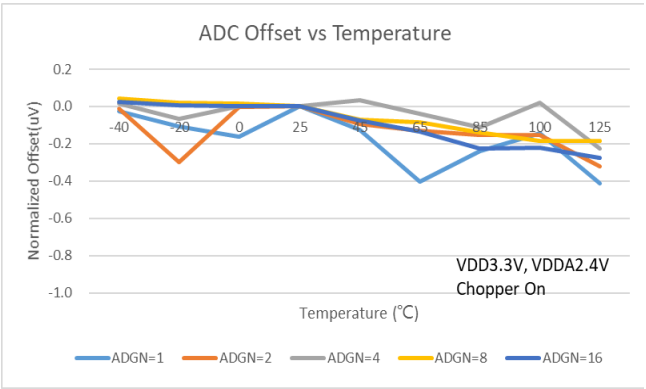


Figure 6.8-1 ADC Offset drift with Temperature

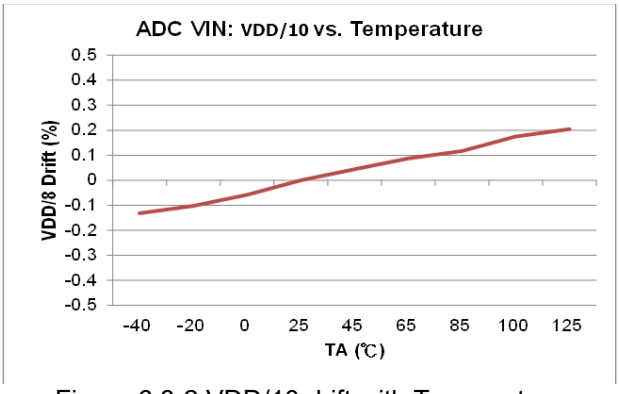


Figure 6.8-2 VDD/10 drift with Temperature

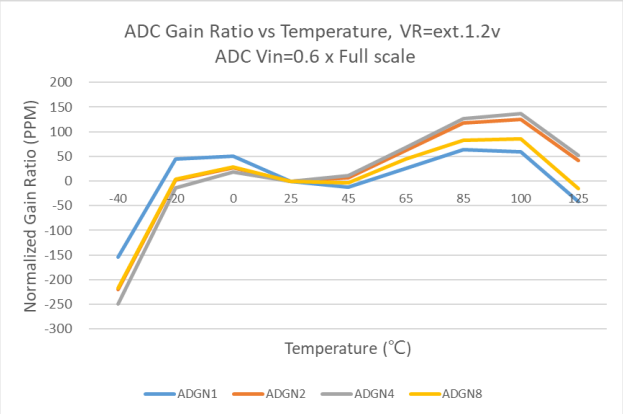


Figure 6.8-3 ADC Gain drift with Temperature

6.8.2. ΣΔADC Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY3123 for ΣΔADC provide important input noise specifications. Table 6.8-4 & 6.8-5 lists typical noise specification sheet and Gain, Output rate, and the largest single-ended input voltage relationship. Test conditions were set at the external input signal is a short circuit, a reference voltage VREF=(VDDA-VSS)/2=1.2V, and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, Vin=VSSA-VSSA, VREF=(VDDA-VSS)/2=1.2V, 2nd conb filter

Max. Vin(mV) =0.9VREF(1)	OSR					32	64	125	250	500	1000	2000	4000	8000	16000	32000	64000
	Output rate(Hz)					31250	15625	8000	4000	2000	1000	500	250	125	63	31	16
	Gain	=	PGAGN	x	ADGN												
±2160	0.25	=	off	x	0.25	10.4	12.2	13.48	15.21	15.79	16.26	16.59	17.14	17.98	18.56	18.98	19.6
±2160	0.5	=	off	x	0.5	10.4	12.21	13.63	15.29	15.81	16.45	17.03	17.49	17.97	18.36	18.98	19.41
±1080	1	=	off	x	1	10.44	12.11	14.14	15.29	15.87	16.36	16.99	17.56	18.01	18.47	18.87	19.41
±540	2	=	off	x	2	10.39	12.18	13.57	15.21	15.9	16.46	16.98	17.47	17.93	18.41	18.86	19.41
±270	4	=	off	x	4	10.38	12.16	13.29	15.22	15.74	16.29	16.88	17.35	17.85	18.33	18.91	19.26
±135	8	=	off	x	8	10.42	12.09	13.49	15.1	15.63	16.19	16.81	17.28	17.86	18.28	18.72	19.09
±68	16	=	off	x	16	10.33	12	13.92	15.01	15.58	16.11	16.68	17.11	17.59	18.14	18.55	19

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, Vin=VSSA-VSSA, VREF=(VDDA-VSS)/2=1.2V, 2nd conb filter, Chopper On

Max. Vin(mV) =0.9VREF(1)	OSR					32	64	125	250	500	1000	2000	4000	8000	16000	32000	64000
	Output rate(Hz)					15625	7813	4000	2000	1000	500	250	125	63	31	16	8
	Gain	=	PGAGN	x	ADGN												
±2160	0.25	=	off	x	0.25	10.89	12.7	14.2	15.88	16.39	16.74	16.83	17.63	18.5	19.07	19.5	20.04
±2160	0.5	=	off	x	0.5	10.8	12.65	14.21	15.66	16.25	16.93	17.38	17.92	18.47	19.01	19.48	20
±1080	1	=	off	x	1	10.85	12.69	14.07	15.66	16.43	16.95	17.49	17.88	18.48	19.04	19.35	20.01
±540	2	=	off	x	2	10.87	12.73	14.2	15.68	16.45	16.85	17.41	18.04	18.41	18.94	19.36	19.91
±270	4	=	off	x	4	10.92	12.72	14.11	15.69	16.2	16.93	17.41	17.95	18.37	18.86	19.46	19.87
±135	8	=	off	x	8	10.85	12.68	14.04	15.52	16.01	16.66	17.39	17.83	18.31	18.8	19.29	19.73
±68	16	=	off	x	16	10.81	12.53	13.88	15.48	16.1	16.63	17.1	17.68	18.06	18.52	19.14	19.48

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

Table6.8-4 ΣΔADC ENOB Table

RMS(uV) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, Vin=VSSA-VSSA, VREF=(VDDA-VSS)/2=1.2V, 2nd conb filter

Max. Vin(mV) =0.9VREF(1)	OSR					32	64	125	250	500	1000	2000	4000	8000	16000	32000	64000
	Output rate(Hz)					31250	15625	8000	4000	2000	1000	500	250	125	63	31	16
	Gain	=	PGAGN	x	ADGN												
±2160	0.25	=	off	x	0.25	7167.72	2052.62	846.32	255.25	170.77	122.81	97.90	66.85	37.35	25.06	18.76	12.19
±2160	0.5	=	off	x	0.5	3585.84	1019.28	380.01	120.90	84.36	53.83	36.00	26.22	18.85	14.33	9.37	6.94
±1080	1	=	off	x	1	1735.51	547.67	133.84	60.37	40.41	28.69	18.53	12.51	9.17	6.64	5.03	3.47
±540	2	=	off	x	2	900.82	259.54	99.46	31.89	19.82	13.37	9.36	6.67	4.85	3.47	2.53	1.73
±270	4	=	off	x	4	453.79	131.66	60.29	15.78	11.03	7.53	4.99	3.61	2.56	1.83	1.22	0.96
±135	8	=	off	x	8	219.94	69.37	26.29	8.58	5.94	4.03	2.64	1.90	1.27	0.95	0.70	0.54
±68	16	=	off	x	16	117.26	36.75	9.75	4.59	3.08	2.14	1.44	1.07	0.76	0.52	0.39	0.29

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

RMS(uV) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, Vin=VSSA-VSSA, VREF=(VDDA-VSS)/2=1.2V, 2nd conb filter, Chopper On

Max. Vin(mV) =0.9VREF(1)	OSR					32	64	125	250	500	1000	2000	4000	8000	16000	32000	64000
	Output rate(Hz)					15625	7813	4000	2000	1000	500	250	125	63	31	16	8
	Gain	=	PGAGN	x	ADGN												
±2160	0.25	=	off	x	0.25	5078.12	1456.73	515.21	159.79	112.25	88.58	83.03	47.74	25.99	17.59	12.99	8.96
±2160	0.5	=	off	x	0.5	2710.97	751.58	255.16	93.61	61.88	38.69	28.29	19.52	13.28	9.18	6.59	4.59
±1080	1	=	off	x	1	1306.67	365.13	140.05	46.81	27.27	19.14	13.14	9.99	6.62	4.48	3.62	2.30
±540	2	=	off	x	2	647.24	178.25	64.25	22.97	13.50	10.24	6.96	4.49	3.46	2.41	1.79	1.23
±270	4	=	off	x	4	312.62	89.41	34.05	11.41	8.04	4.85	3.46	2.38	1.79	1.27	0.84	0.63
±135	8	=	off	x	8	163.64	45.95	17.88	6.44	4.57	2.91	1.76	1.30	0.93	0.66	0.47	0.35
±68	16	=	off	x	16	83.87	25.55	10.02	3.31	2.14	1.49	1.07	0.72	0.55	0.40	0.26	0.21

Table 6.8-5 ΣΔADC RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$ENOB(RMS) = \ln\left(\frac{FSR}{RMS\ Noise}\right) \Big/ \ln(2)$$

$$RMS\ Noise = \left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right) \Big/ 2^{23}$$

Where FSR (Full - Scale Range) $= 2 \times$ VREF/Gain.

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

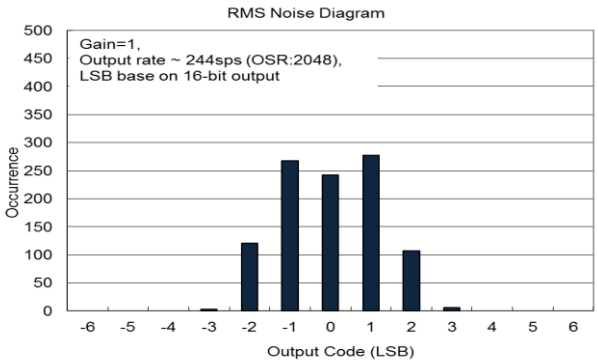


Figure 6.8-1 RMS Noise Diagram

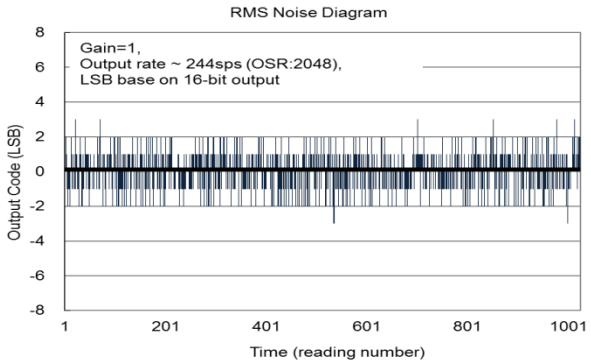


Figure 6.8-2 Output Code Diagram

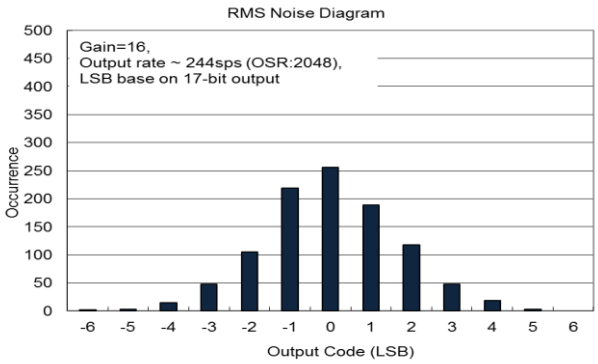


Figure 6.8-3 RMS Noise Diagram

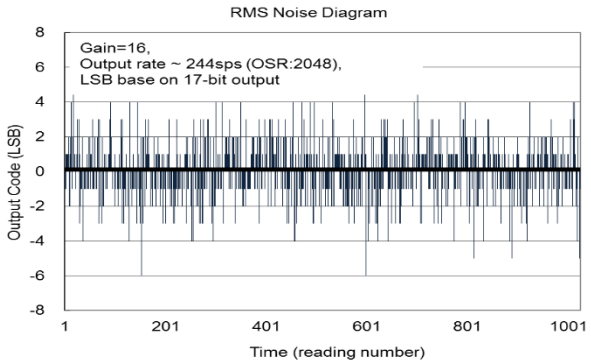


Figure 6.8-4 Output Code Diagram

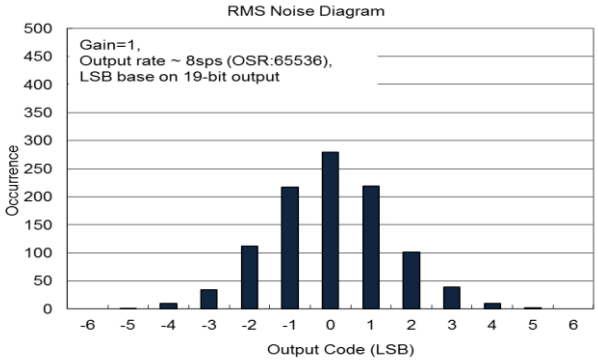


Figure 6.8-5 RMS Noise Diagram

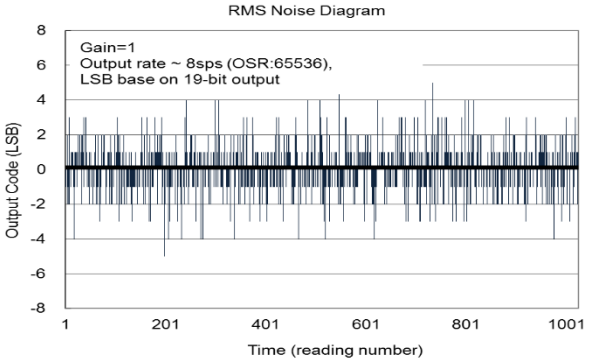


Figure 6.8-6 Output Code Diagram

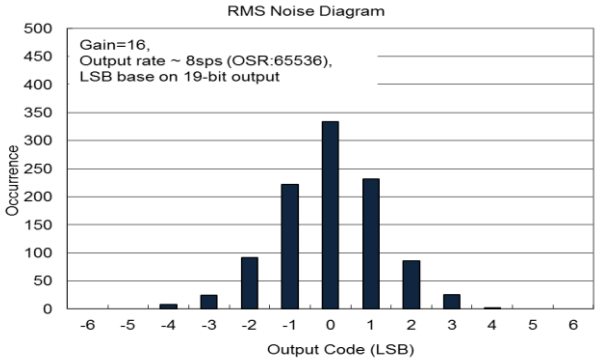


Figure 6.8-7 RMS Noise Diagram

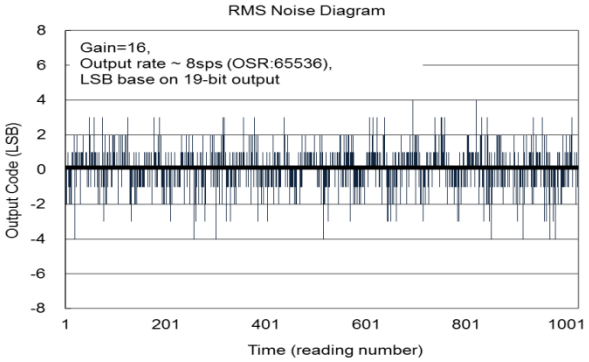


Figure 6.8-8 Output Code Diagram

6.8.3. ΣΔADC Temperature Sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute Temperature Scale 0°K			-272		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

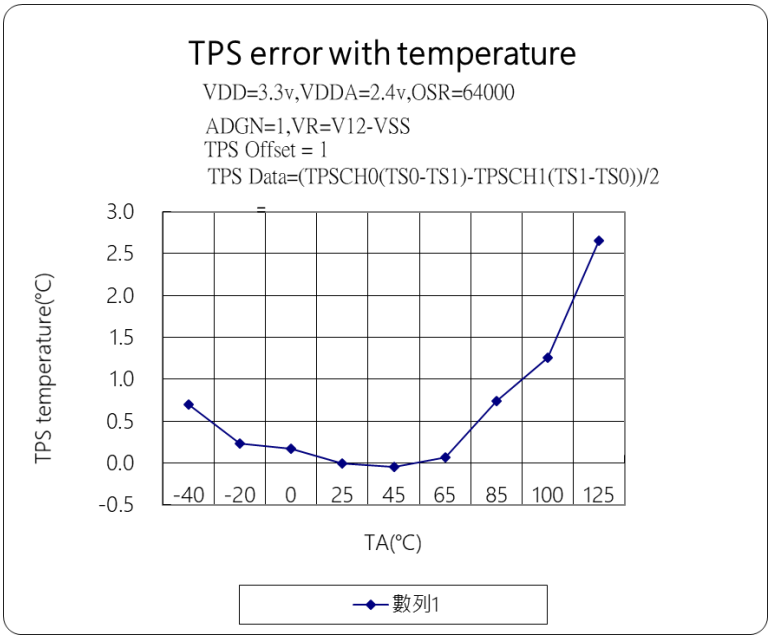


Figure 6.8-9 TPS Temperature Error

6.9. Rail to Rail OPAMP1、OPAMP2、OPAMP3

T_A = 25℃,V_{DD3V} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power supply		2.2		3.6	V
V_{OUT}	Output range		0		VDDA	V
V_{IN}	Input common range		0		VDDA	V
I_{OPA}	OPAMP current			360		uA
I_{OPA_LOAD}	Output current loading (push or pull)	VDDA = 3.0V, 0.3V< Output voltage <VDDA-0.3V			1	mA
		VDDA = 2.4V, 0.3V< Output voltage <VDDA-0.3V			0.5	mA
C_{LOAD}	Max output capacitor load				1	nF
SR	Slew rate	Loading R=10K, C=100pF, 0.3V → VDDA-0.3V		0.6		V/uS
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
V_{OS}	Offset error	Vin = 1.2V	-5		+5	mV
DFD	Digital filter delay	VDDA = 3.0V		2		uS
C_{SA}	Sample capacitor			10		pF

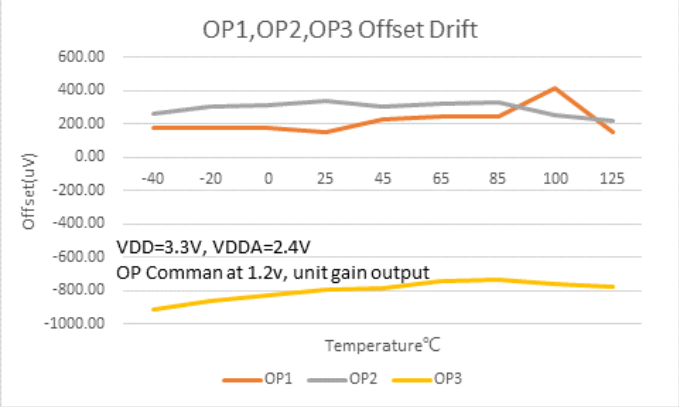
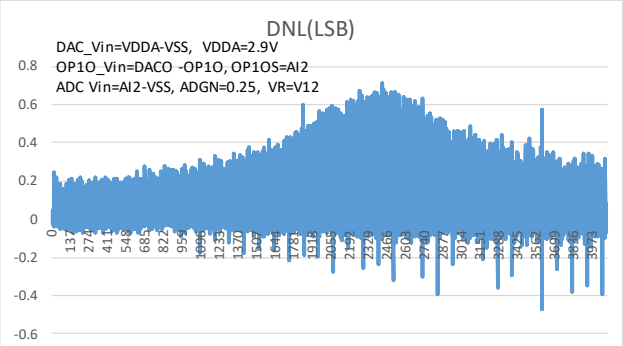


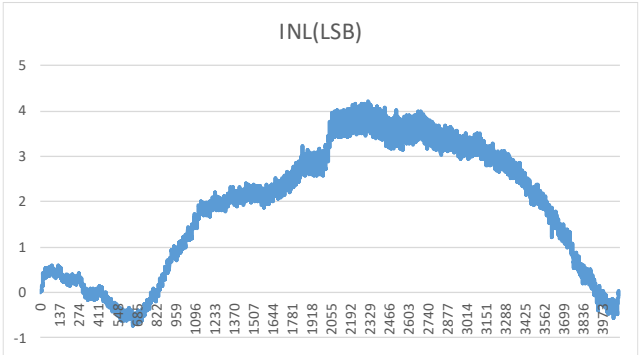
Figure 6.9-1 R2ROPAMP Offset Temperature

6.10. 12-Bit Resistance Ladder

Typical values are at T_A=25℃ and VDD = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Resolution		Monotonic		12		Bit
	Power Supply		2.2		VDDA	V
	Operation current			50		uA
V_{OUT}	Output range	Output is between Vrefp and Vrefn	0		VDDA	V
V_{REFP}	Positive reference voltage range	$V_{REFP} > V_{REFN}$	0		VDDA	V
V_{REFN}	Negative reference voltage range		0		VDDA	V
R_{LADDER}	One LSB resistance ladder			200		Ω
INL	Integral linearity error	Vrefp = 2.4V, Vrefn = 0V		±3	±6	LSB
DNL	Differential linearity error	Vrefp = 2.4V, Vrefn = 0V		±1	±2	LSB
E_{OS}	Offset error	Vrefp = 2.4V, Vrefn = 0V			1	LSB





6.11. BIA Module

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IAM1	Active mode 1	HAO =8.5MHz, CPU_CK =8.5MHz VDDA=2.4V、ENADC、ENACM ADC_CK=8.5M/8 SinWave=50K Vpp=200mV		1840		uA
HAO：Internal High Accuracy Oscillator frequency.						

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Err1	S.D/Average	(10K//1nF)//10K SinWave=5K Vpp=200mV			0.1	CV
Err2		(10K//1nF)//10K SinWave=10K Vpp=200mV			0.1	CV
Err3		(100K//1nF)//100K SinWave=5K Vpp=200mV			0.1	CV
Err4		(100K//1nF)//100K SinWave=10K Vpp=200mV			0.1	CV
S.D：standard deviation						

7. I²C Communication Protocol

- Support ADC IRQ vector (CLKOUT PIN)
- f_{SCL}=400KHz
- The chip's slave address is defined as 0xA0h

The chip address is fixed at 0xA0, which is device address[6:0] = 1010000b.

The communication method adopts the flexible I²C architecture, and can be planned to have IRQ notification or no IRQ notification after the ADC conversion is completed to achieve different application modes. When the communication protocol is set in the no IRQ mode, the read time for the ADC conversion completion must be calculated by the user. The user can read the state of the register ADCL[ADST] to determine whether the ADC output data has been read.

When the communication protocol is set in IRQ mode, then the IRQ signal output will be generated after the ADC conversion is completed, and the IRQ will output the change through the CLKOUT or SDA pin. When this mode is set, the pin output will be at a high potential, and the ADC conversion is completed. After that, the output will generate a low potential or a low pulse signal at the pin position to achieve the purpose of notifying the user. When the IRQ is set to the SDA multiplexed output, when the ADC conversion is completed and the IRQ interrupt needs to be triggered, if the I²C communication is in progress, the output state of the SDA will occur after the I²C Stop.

The I²C supports the General Call Reset function. When the chip receives the Reset command, it will reset the control register. Except for the data in the HAOTRIM register and SRAM, the rest of the address data will be restored to the state after the BOR. For related status, refer to the "I²C RST" field in the register list of chaper 5.

The 07Fh command is reserved for switching between different bank blocks. When accessing the waveform data register, you need to switch the correct bank settings. When the setting data is 0, the Bank 0 block data is accessed; when the setting data is 1, the Bank 1 block data is accessed. When accessing the waveform data from point 1 to point 64, use Bank 0 space 080h~0FFh; when accessing waveform data from point 65 to point 128, use Bank 1 space 180h~1FFh;

7.1. I²C Communication Sequence Diagram

The HY3123 I²C slave communication format is illustrated in the following figure, which is subdivided into:

a. Valid Data Definition
b. Start and Stop Definition
c. MACK Definition
d. IRQ Definition
e. Wave Definition
f. Write Register
g. Read Register
h. Reread Register
i. Write Register then Read Register
j. General Call Reset

Valid Data Definition

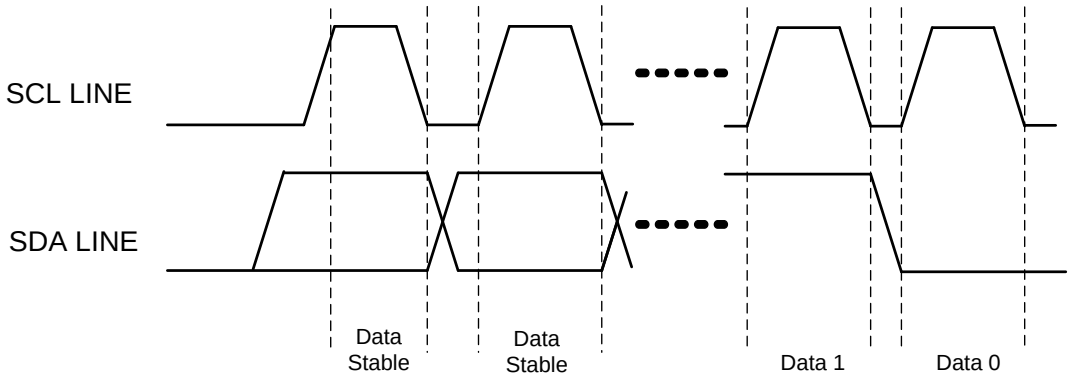


Figure 7-1 Valid Data Waveform

Start and Stop Definition

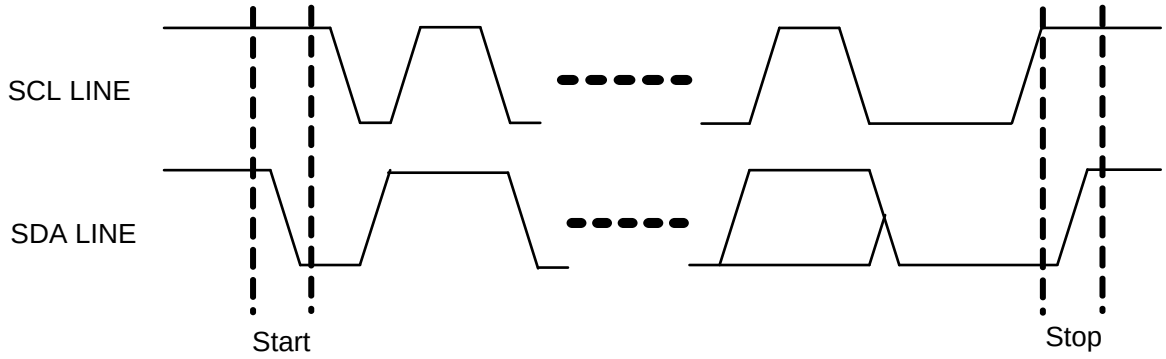
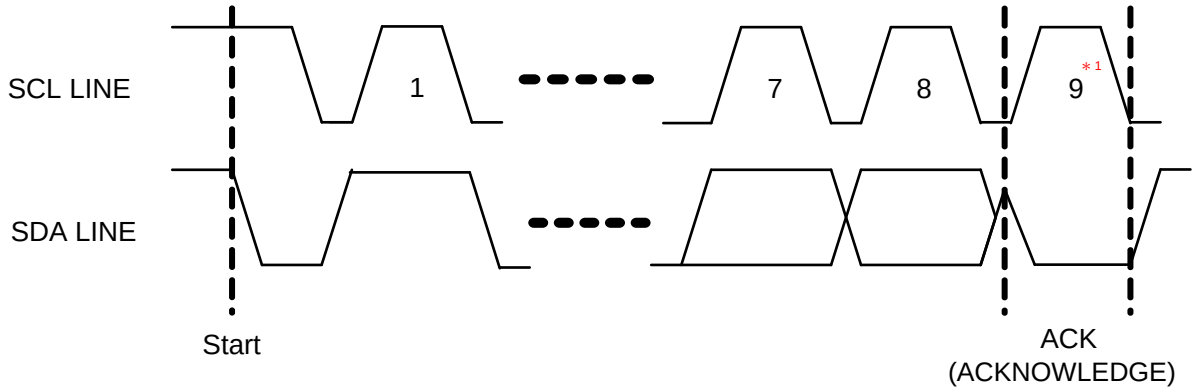


Figure 7-2 Start and Stop Waveform

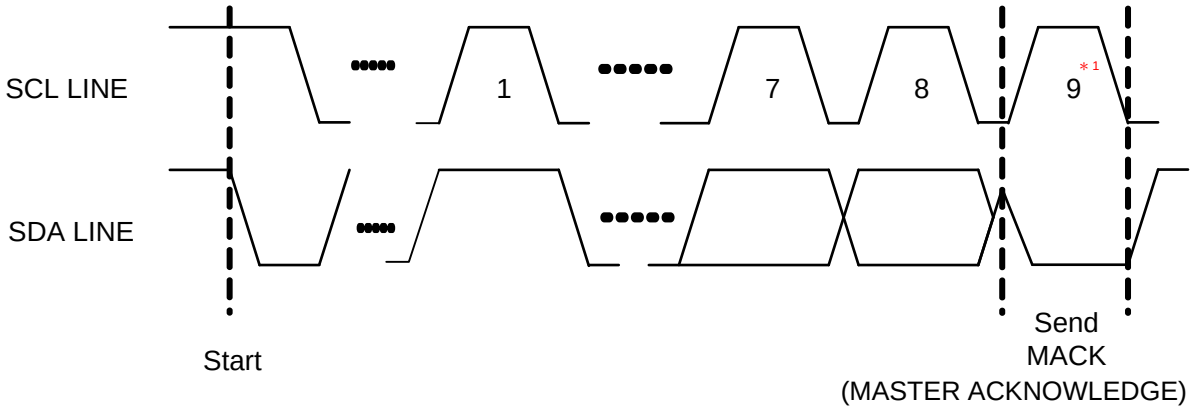
ACK Definition



*1. When the master sends the SCL signal to the 8th clock to the slave, the output is set to Low (ACK), and the SDA pin of the master must be changed from the output state to the input state to receive The response signal generated by the slave.

Figure 7-3 Acknowledge(ACK) Signal Waveform

MACK Definition



*1. MACK occurs when continuously reading Multi bytes data output. Before the second data is to be output, the SDA must be controlled by the Master before the 9th CLOCK rising edge. The output is set to Low(ACK), informs the Slave to continue to output the data after the second pen.

Figure 7-4 Continuous reading of the transmitted signal waveform (MACK)

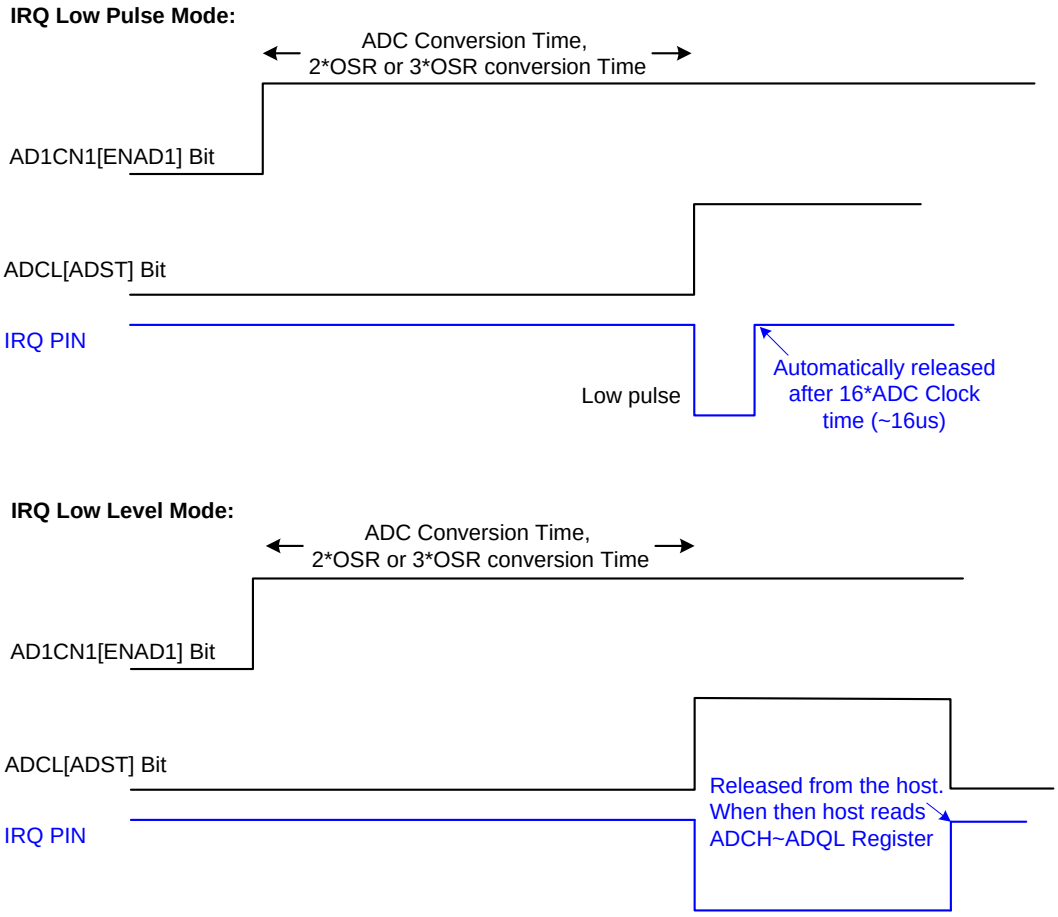


Figure 7-4 Interrupt Request Signal Waveform (IRQ)

Wave Definition

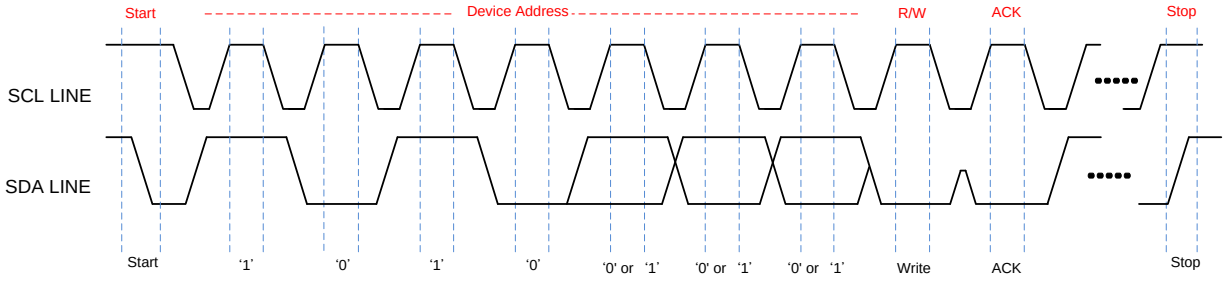
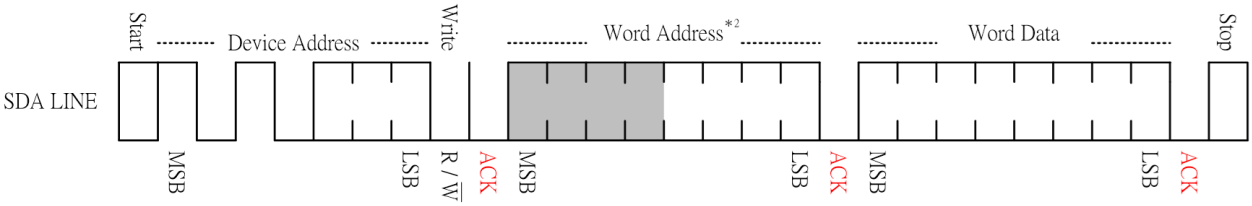


Figure 7-5 Waveform Definition

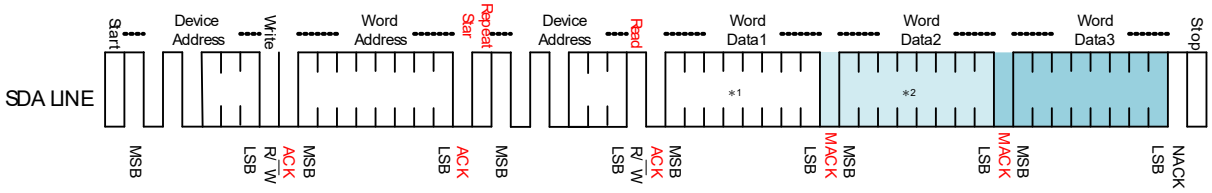
Write Register



*2 Word Address: Reserved 0x7F is used to switch Bank special command; and the user avoids invalid operation address, will not get ACK response, you must first Stop and then restart Star to continue communication.

Figure 7-6 Write Register

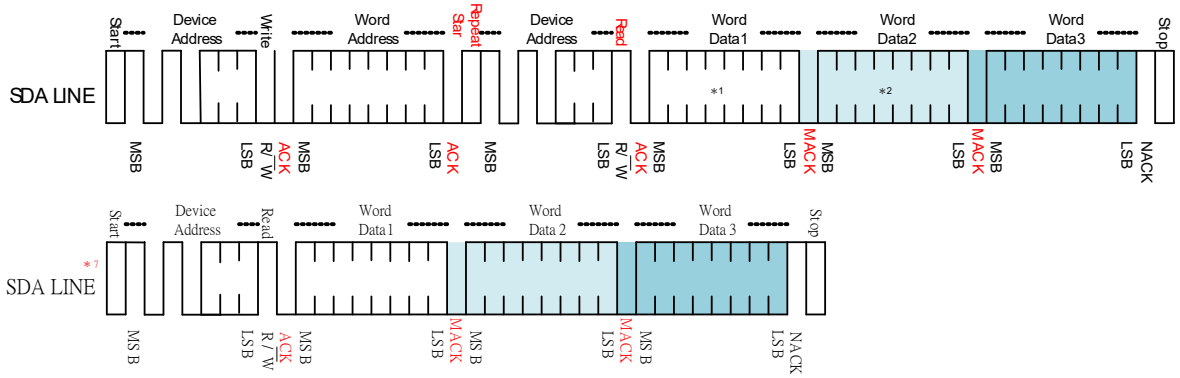
Read Register



*1. When reading a single Address data, the returned data is only Word Data1.
*2. To read consecutive Address data, such as ADCH~ADCL, the data returned is Word Data1 + Word Data2+ Word Data3. When it is necessary to return Data2/Data3 data, the MACK must be set to Low by the host.

Figure 7-8 Read Register

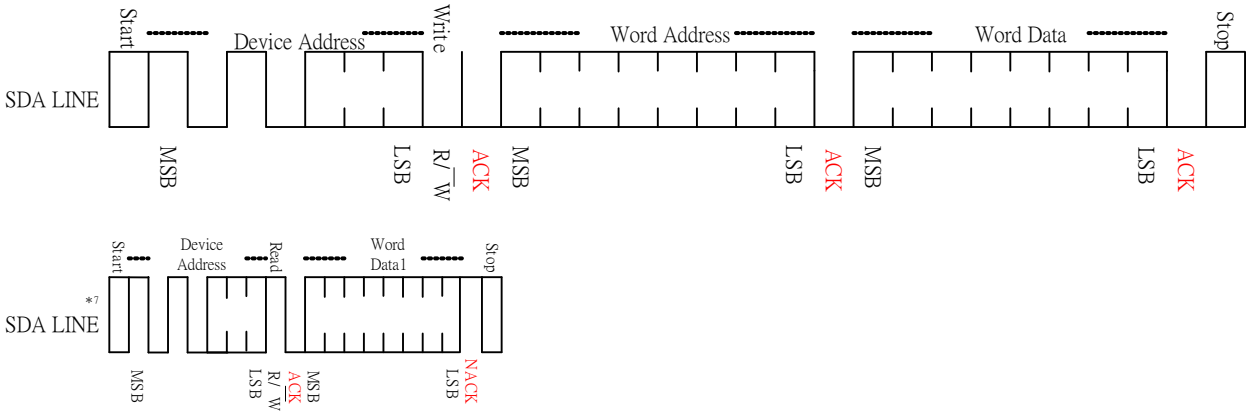
Reread Register



*7. When the specified Word Address is read, it can be read without re-specifying Word Address when reading again.

Figure 7-9 Reread Register

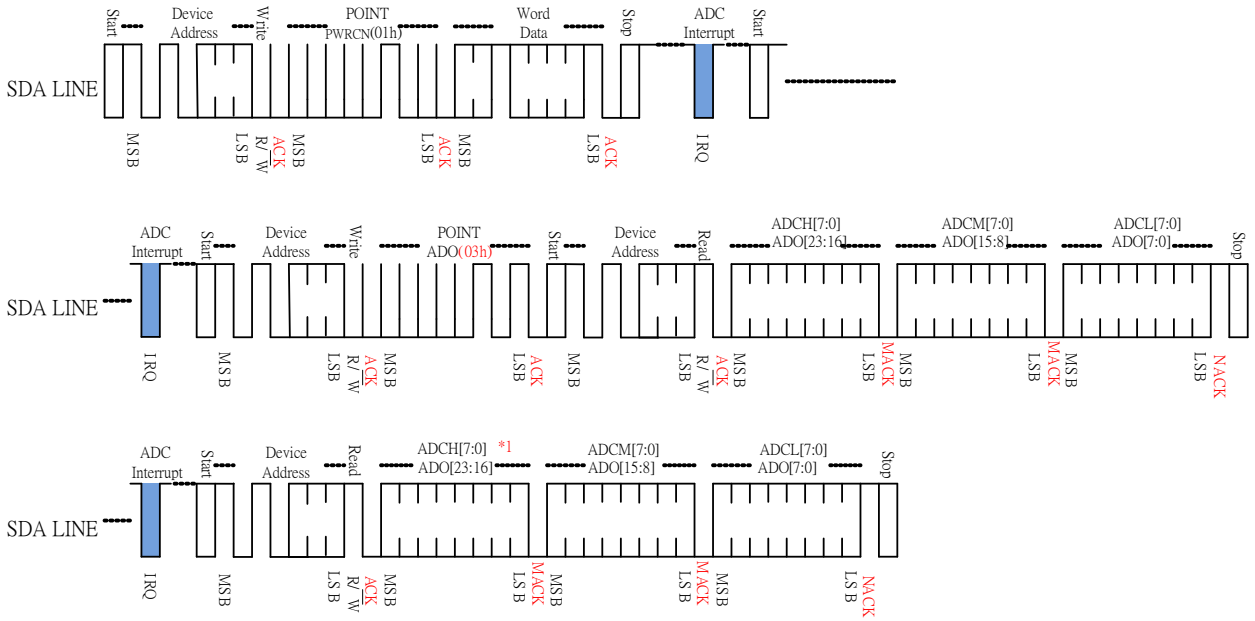
Write Register then Read Register



*7. When Word Data of the specified Word Address is written, and then read, you do not need to specify Word Address again to read it.

Figure 7-10 Repeated confirmation after Write to Register

Interrupt IRQ's ADC register read



*1. When the POINT address is 03H=ADCH[7:0], or 06H=ADIH[7:0], the data continuous reading function can be supported, and the POINT Address does not need to be re-read when re-reading.

Figure 7-11 Interrupt IRQ's ADC register read

Call Chip Reset

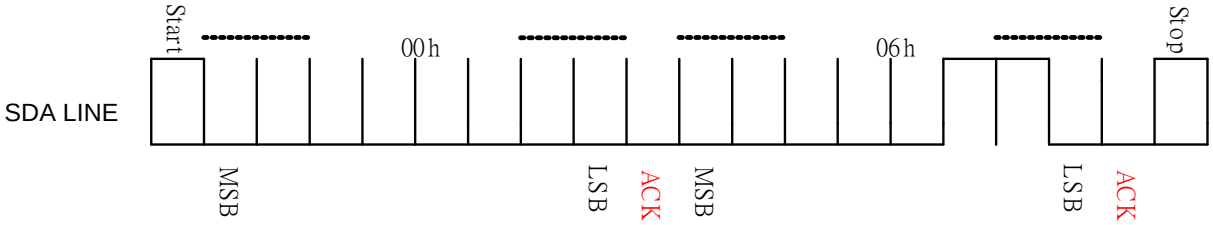
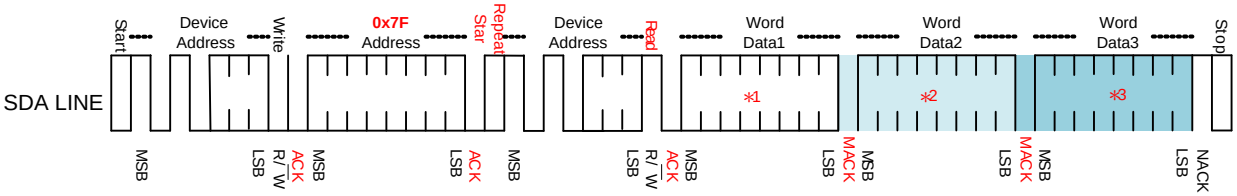


Figure 7-12 General Call Reset

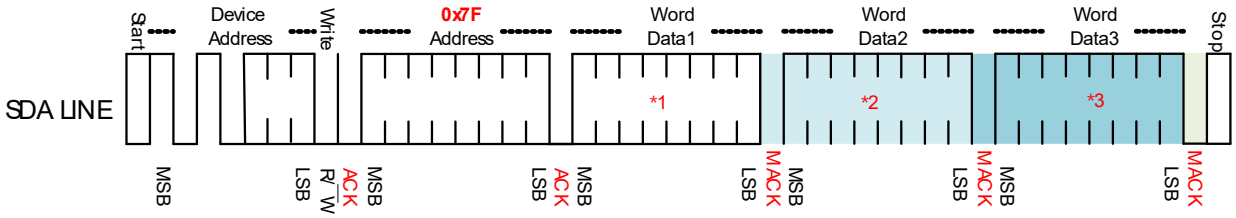
SRAM Register Read



*1. When operating SRAM bank0, 0x80~0xFF interval, you need to set Word Data1=0x00;
When operating SRAM bank1, 0x180~0x1FF interval, you need to set Word Data1=0x01;
When you want to operate the SRAM data, you need to switch the correct bank before you can write the data correctly.
*2. Word Data2 represents the operation SRAM 0x80, which represents the first data of the waveform output High byte.
*3. Word Data2 represents the operation SRAM 0x81, which represents the first data of the waveform output Low byte.

Figure 7-13 SRAM register Read (0x7F special command switch Bank)

SRAM Register Write



*1. When operating SRAM bank0, 0x80~0xFF interval, you need to set Word Data1=0x00;
When operating SRAM bank1, 0x180~0x1FF interval, you need to set Word Data1=0x01;
When you want to operate the SRAM data, you need to switch the correct bank before you can write the data correctly.
*2. Word Data2 represents the operation SRAM 0x80, which represents the first data of the waveform output High byte.
*3. Word Data2 represents the operation SRAM 0x81, which represents the first data of the waveform output Low byte.
4. Need to end the write process through the Stop command.

Figure 7-14 SRAM register Write (0x7F special command switch Bank)

8. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY3123-ES20	SSOP	20	E	S20	000	Tube	58	Green[4]	MSL-3
HY3123-ES20	SSOP	20	E	S20	000	Tape & Reel	3000	Green[4]	MSL-3
HY3123-E016	SSOP	16	E	016	000	Tube	100	Green[4]	MSL-3
HY3123-E016	SSOP	16	E	016	000	Tape & Reel	2500	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code (Blank Code/ Standard/Customized Programming Code)**

Ex: You request in SSOP16 package. The device No. will be HY3123-E016 and please clearly indicate the shipment packing type when placing orders.

[2] **Code:**

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

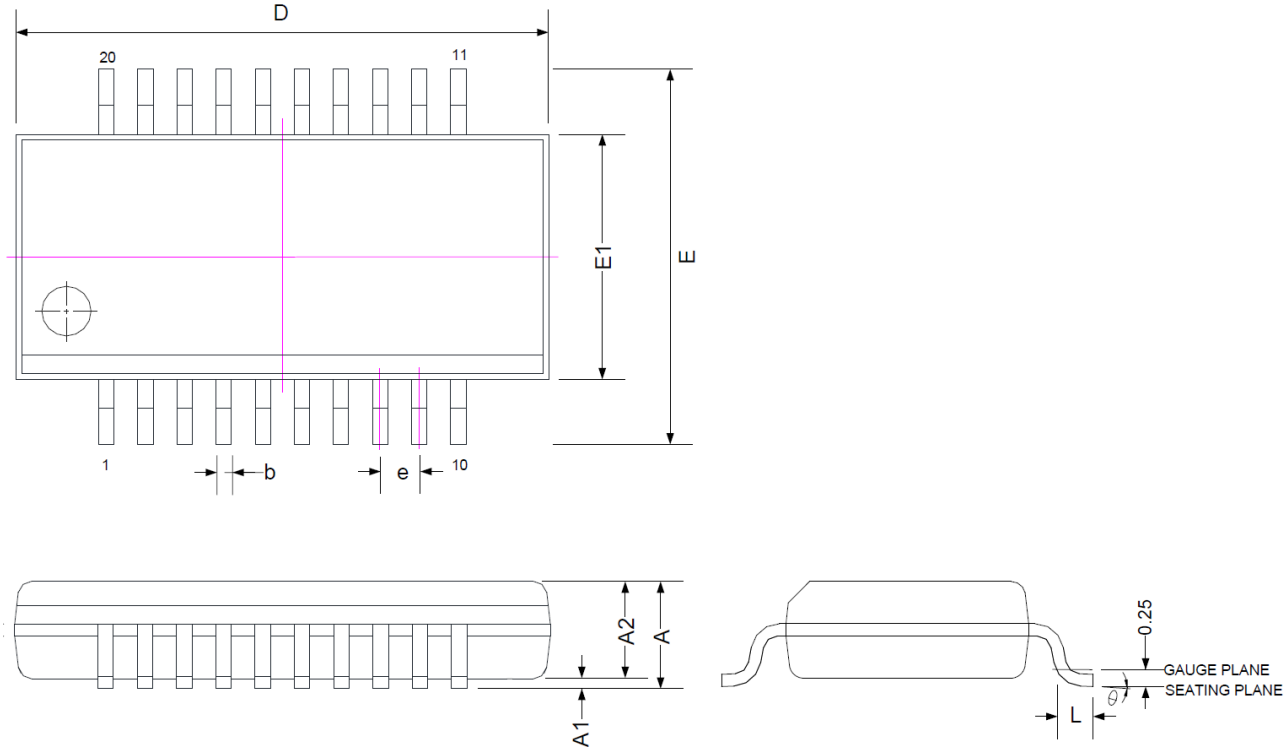
[4] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm).

9. Packaging Information

9.1. SSOP20(ES20)

9.1.1. Package Dimensions SSOP20(150mil)

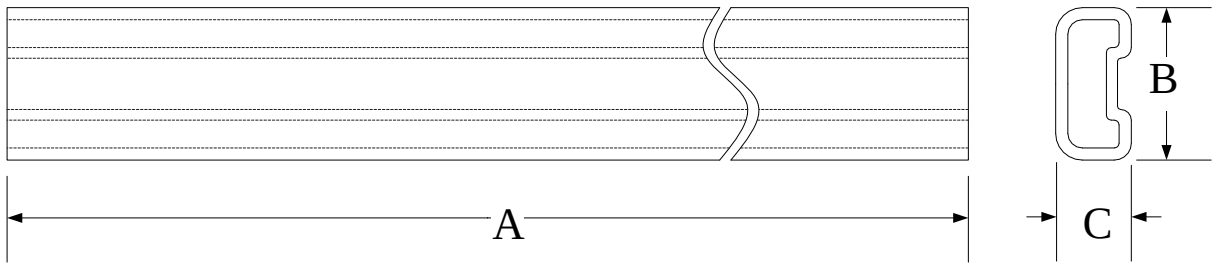


SYMBOLS	MIN	NOM	MAX
A	1.34	1.63	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	8.55	8.66	8.74
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	0.64	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:
1. All dimensions refer to JEDEC OUTLINE MS-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

9.1.2. Tube Dimensions SSOP20(150mil)

Unit : mm

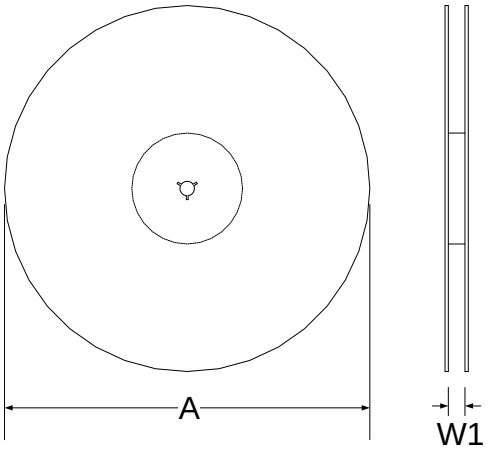


SYMBOLS	A	B	C
Spec.	529.6±1.0	8.001±0.127	3.937±0.127

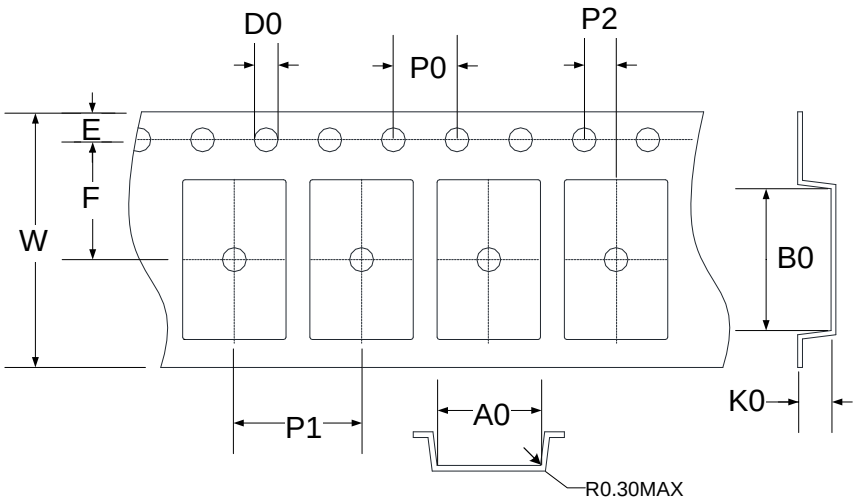
9.1.3. Tape & Reel Information

9.1.3.1. Reel Dimensions

Unit: mm



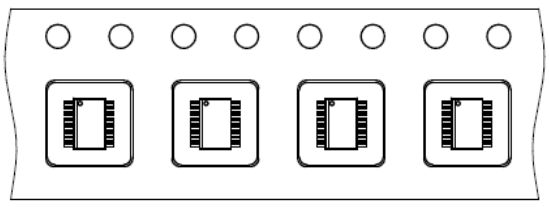
9.1.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	9.50	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

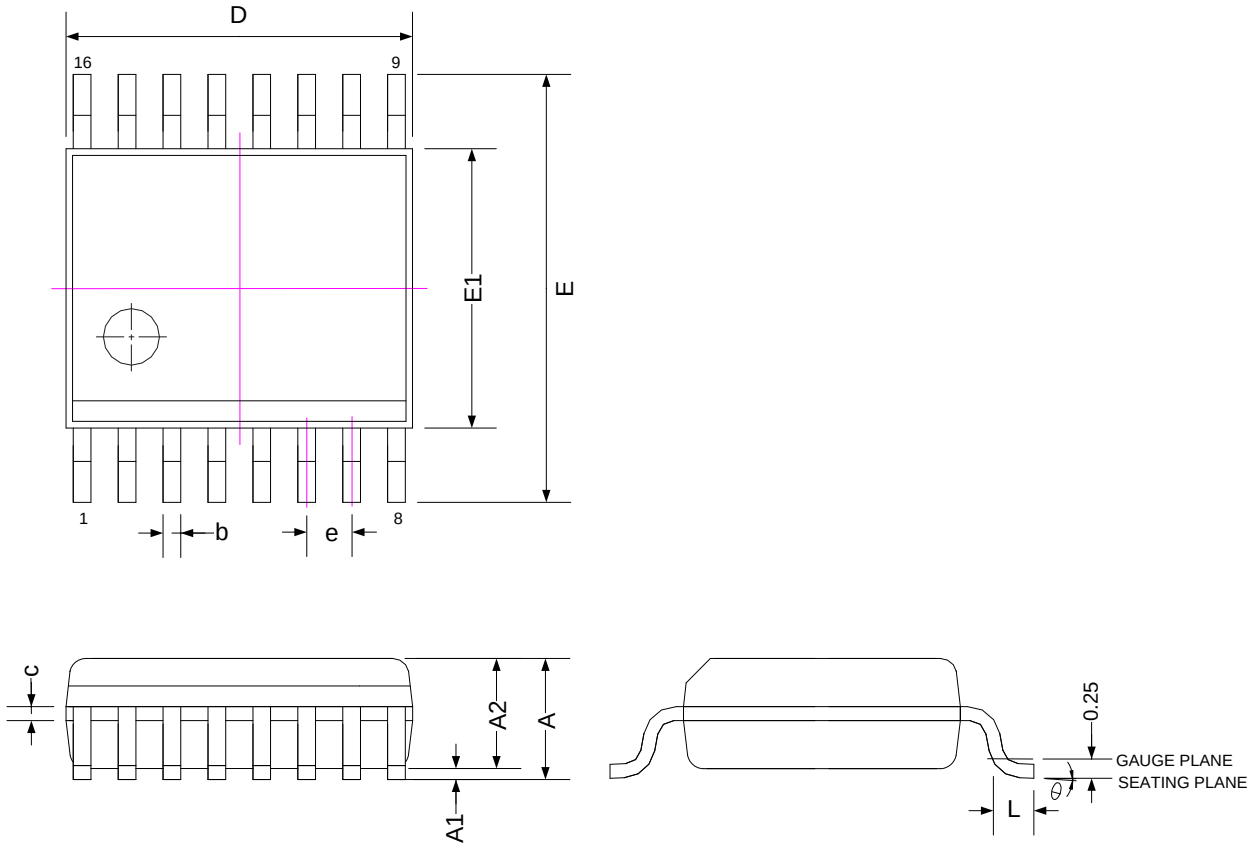
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

9.1.3.3. Pin1 direction



9.2. SSOP16(E016)

9.2.1. Package Dimensions SSOP16(150mil)



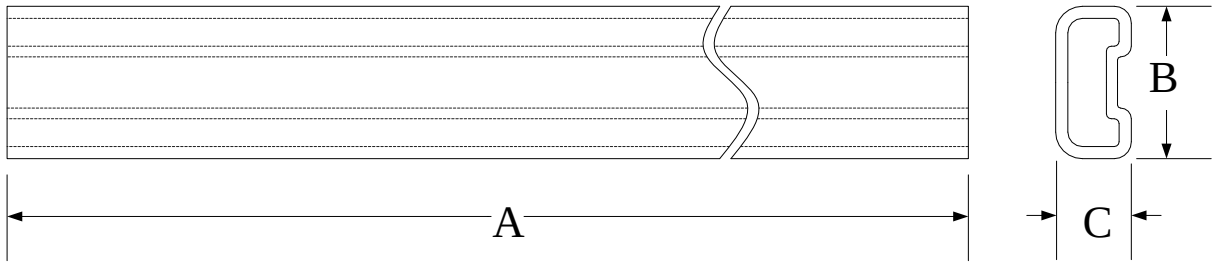
SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	4.80	4.90	5.00
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	-	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

9.2.2. Tube Dimensions SSOP16(150mil)

Unit : mm



Type 1:

SYMBOLS	A	B	C
Spec.	521.0±1.0	7.747±0.15	3.810±0.15

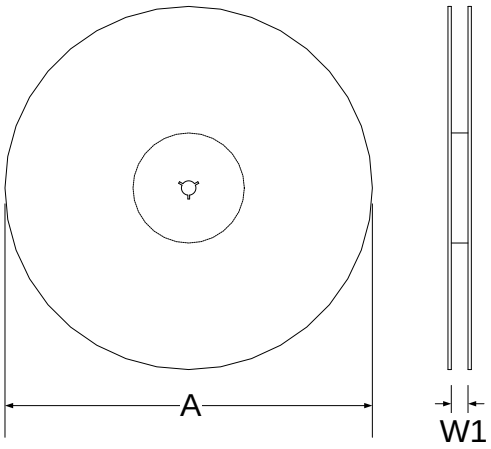
Type 2:

SYMBOLS	A	B	C
Spec.	521.0±1.0	7.874 REF.	3.810 REF.

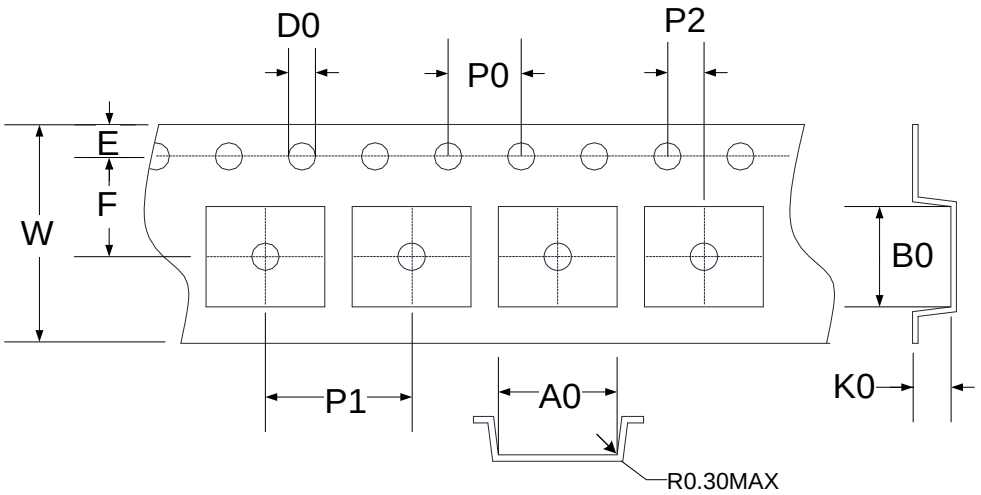
9.2.3. Tape & Reel Information

9.2.3.1. Reel Dimensions-Type1

Unit: mm



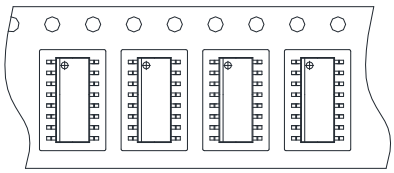
9.2.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.90	5.40	2.00	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

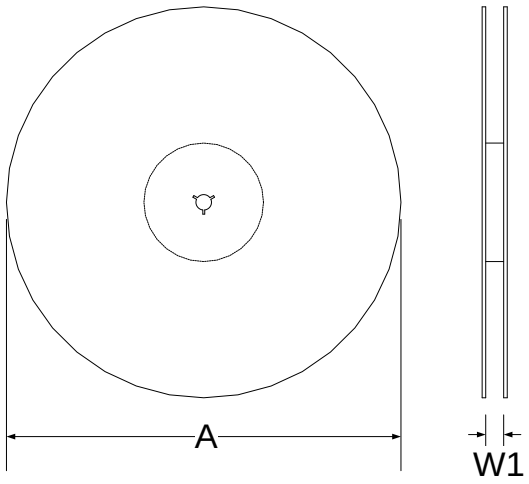
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.
Unit : mm

9.2.3.3. Pin1 direction

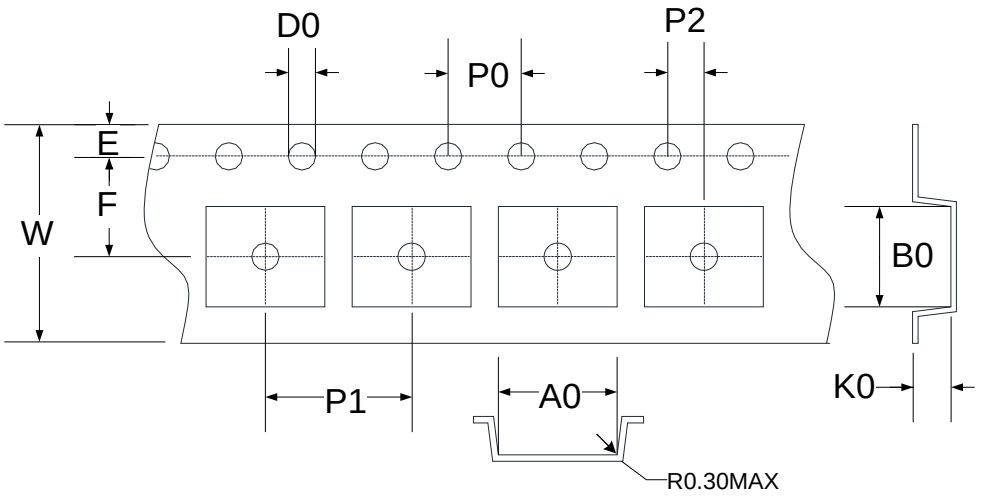


9.2.3.4. Reel Dimensions-Type2

Unit: mm



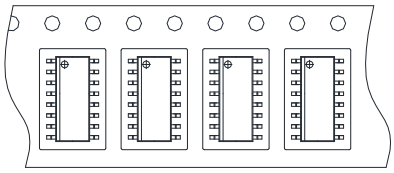
9.2.3.5. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.50	5.20	2.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.
Unit : mm

9.2.3.6. Pin1 direction



10. Revision Record

Major differences are stated thereinafter.

Version	Page	Date	Revision Summary
V01	All	2019/02/27	First edition
V02	All	2019/10/16	Adding packaging SSOP20 Update electrical characteristic
V03	19、22	2021/02/05	Update register table
	18		Update IRQ instructions
	17		Update ENBGR instructions
	44		Update R2ROP characteristic
	15、25~28		Update R2ROP register name
	15、30		Adding RAMBANK register
	20		Update One shot mode instructions
	37		Update VDDA、REFO、ACM characteristic
	52		Update SSOP20 Unit Q'ty
V04	All	2022/08/10	Modify register description to match current situation
V05	13 41 48	2023/09/14	1. Modify NC pin description 2. Corrected Avg/S.D to S.D/Average 3. Modify the individual package quantity of the Tape & Reel shipping packaging of the HY3123-ES20 product to 3000
V06	41	2024/03/07	Corrected Linearity error specification of INL & DNL in Chapter 6.10
	All	2024/04/01	Update the VDDA voltage range to 2.4V~3.6V
V07	All	2024/05/09	Three new VDDA voltage levels are added: 2.2V, 2.25V, and 2.3V. VDDA voltage range updated to 2.2V~3.6V